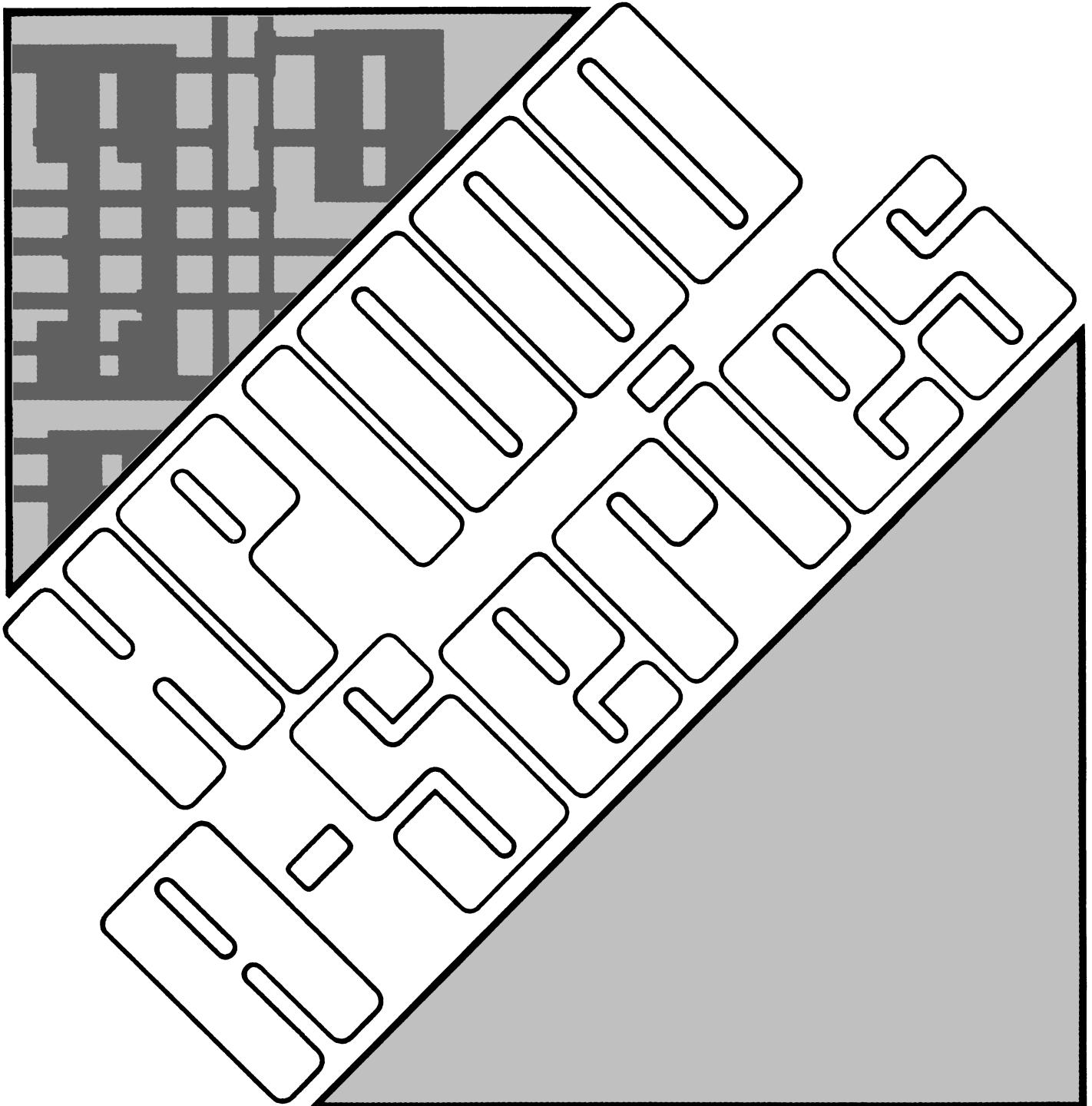


HP 12006A Parallel Interface

Reference Manual



HP 1000 L/A-Series Computer Systems

HP 12006A Parallel Interface

Reference Manual

Card Assembly: 12006-60003
Date Code: A-2350

Backdating information for

Card Assembly: 12006-60002
Date Code: All
Card Assembly: 12006-60001
Date Code: B-2001



HEWLETT-PACKARD COMPANY
Roseville Networks Division
8000 Foothills Boulevard
Roseville, California 95678

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PRINTING HISTORY

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12006-90001

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SAFETY CONSIDERATIONS

GENERAL - This product and related documentation must be reviewed for familiarization with safety markings and instructions before operation.

SAFETY SYMBOLS



Instruction manual symbol: the product will be marked with this symbol when it is necessary for the user to refer to the instruction manual in order to protect the product against damage.



Indicates hazardous voltages.



Indicates earth (ground) terminal (sometimes used in manual to indicate circuit common connected to grounded chassis).

WARNING

The **WARNING** sign denotes a hazard. It calls attention to a procedure, practice, or the like, which, if not correctly performed or adhered to, could result in injury. Do not proceed beyond a **WARNING** sign until the indicated conditions are fully understood and met.

CAUTION

The **CAUTION** sign denotes a hazard. It calls attention to an operating procedure, practice, or the like, which, if not correctly performed or adhered to, could result in damage to or destruction of part or all of the product. Do not proceed beyond a **CAUTION** sign until the indicated condi-

When handling or servicing equipment containing static sensitive devices, adequate precautions must be taken to prevent device damage or destruction. Only those who are thoroughly familiar with industry accepted techniques for handling static sensitive devices should attempt to service the cards with these devices. In all instances, measures must be taken to prevent static charge buildup on work surfaces and persons handling the devices. Cautions are included through this manual where handling and maintenance involve static sensitive devices.

SAFETY EARTH GROUND - This is a safety class I product and is provided with a protective earthing terminal. An uninterruptible safety earth ground must be provided from the main power source to the product input wiring terminals, power cord, or supplied power cord set. Whenever it is likely that the protection has been impaired, the product must be made inoperative and be secured against any unintended operation.

BEFORE APPLYING POWER - Verify that the product is configured to match the available main power source per the input power configuration instructions provided in this manual.

If this product is to be energized via an auto-transformer (for voltage reduction) make sure the common terminal is connected to the earth terminal of the main power source.

SERVICING

WARNING

Any servicing, adjustment, maintenance, or repair of this product must be performed only by qualified personnel.

Adjustments described in this manual may be performed with power supplied to the product while protective covers are removed. Energy available at many points may, if contacted, result in personal injury.

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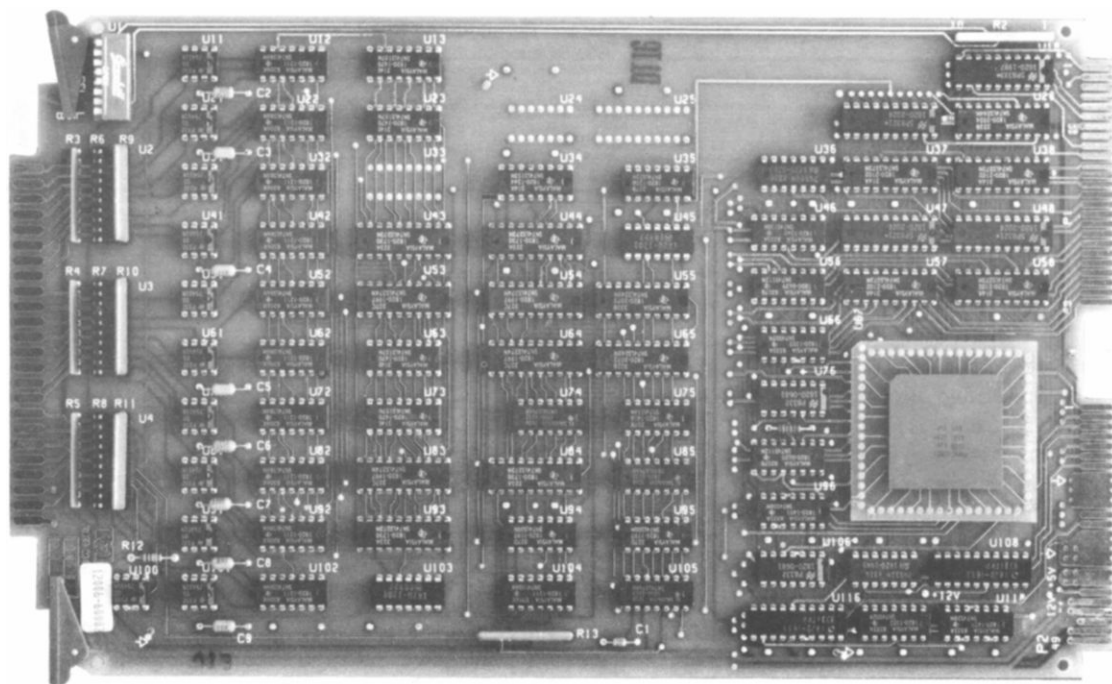


Figure 1-1. HP 12006A Parallel Interface

INTRODUCTION

SECTION

I

1-1. INTRODUCTION

This manual provides general information, installation, programming instructions, theory of operation, maintenance instructions, replaceable parts information, and servicing diagrams for the Hewlett-Packard HP 12006A Parallel Interface.

1-2. DESCRIPTION

1-3. GENERAL

The HP 12006A is a multi-purpose parallel interface for the HP 1000 A/L-Series Computer. The parallel interface provides the capability for 8- or 16-bit bi-directional, high-speed transfers of data. A simplified block diagram of the parallel interface is shown in figure 1-2. The Parallel Interface Card (PIC) plugs into a single slot in the A/L-Series backplane (see figure 1-3) and is assigned exactly one select code.

The card may be connected by cable to from one to 16 devices, or to another parallel interface card (for computer-to-computer communications). Besides including registers for 16-bit bi-directional transfers, the parallel interface has a 4-bit command and a 4-bit status register so that it can control varied operations of a particular device, or interface to an intelligent device. The card may connect to +5 (TTL) or +12 volt devices. Thus, the parallel interface card is a multi-purpose input/output (I/O) card.

The parallel interface has the capability of handling its own memory accesses (Direct Memory Access (DMA)), and of decoding its own instructions from the central processor unit (CPU). These features are performed by interface logic and an I/O processor integrated circuit (chip). This I/O chip and interface logic is referred to as the "I/O master." The I/O master is located on the card and performs all functions (instruction recognition and DMA control) necessary for interfacing with the backplane. Figure 1-4 shows the parallel interface card in a typical L-Series system environment.

1-4. EQUIPMENT SUPPLIED

The standard HP 12006A Parallel Interface consists of the following items:

- a. Parallel Interface Card, part no. 12006-60003.

- b. 48-pin Connector Kit, part no. 5061-3426.
- c. Parallel Interface Reference Manual, part no. 12006-90001.

1-5. IDENTIFICATION

1-6. PRODUCT. Five digits and a letter (12006A in this case) are used to identify Hewlett-Packard products used with HP computers. The five digits identify the product, the letter indicates the revision level of the product.

1-7. CIRCUIT CARD. The circuit card is identified by a part number marked on the card. In addition to the part number, the card is further identified by a letter and a date code consisting of four digits (e.g., A-2350). This designation is placed below the part number. The letter identifies the version of the etched circuit on the card. The date code (the four digits following the letter) identifies the electrical characteristics of the card with components mounted. Thus, the complete part number on the parallel interface card could be:

12006-60003
A-2350

If the assembly number stamped on the parallel interface card does not agree with the assembly number on the title page of this manual, there are differences between your card and the card described herein. These differences are described in manual supplements available at the nearest Hewlett-Packard Sales and Service Office (a list of Hewlett-Packard Sales and Service Offices is contained at the back of this manual).

1-8. REFERENCE MANUAL. The manual is identified by its name and part number. The part number, 12006-90001, is printed on the title page. The publication date also is printed on the title page. If the manual is revised, the publication date is changed.

1-9. SPECIFICATIONS

Table 1-1 lists the specifications of the HP 12006A Parallel Interface.

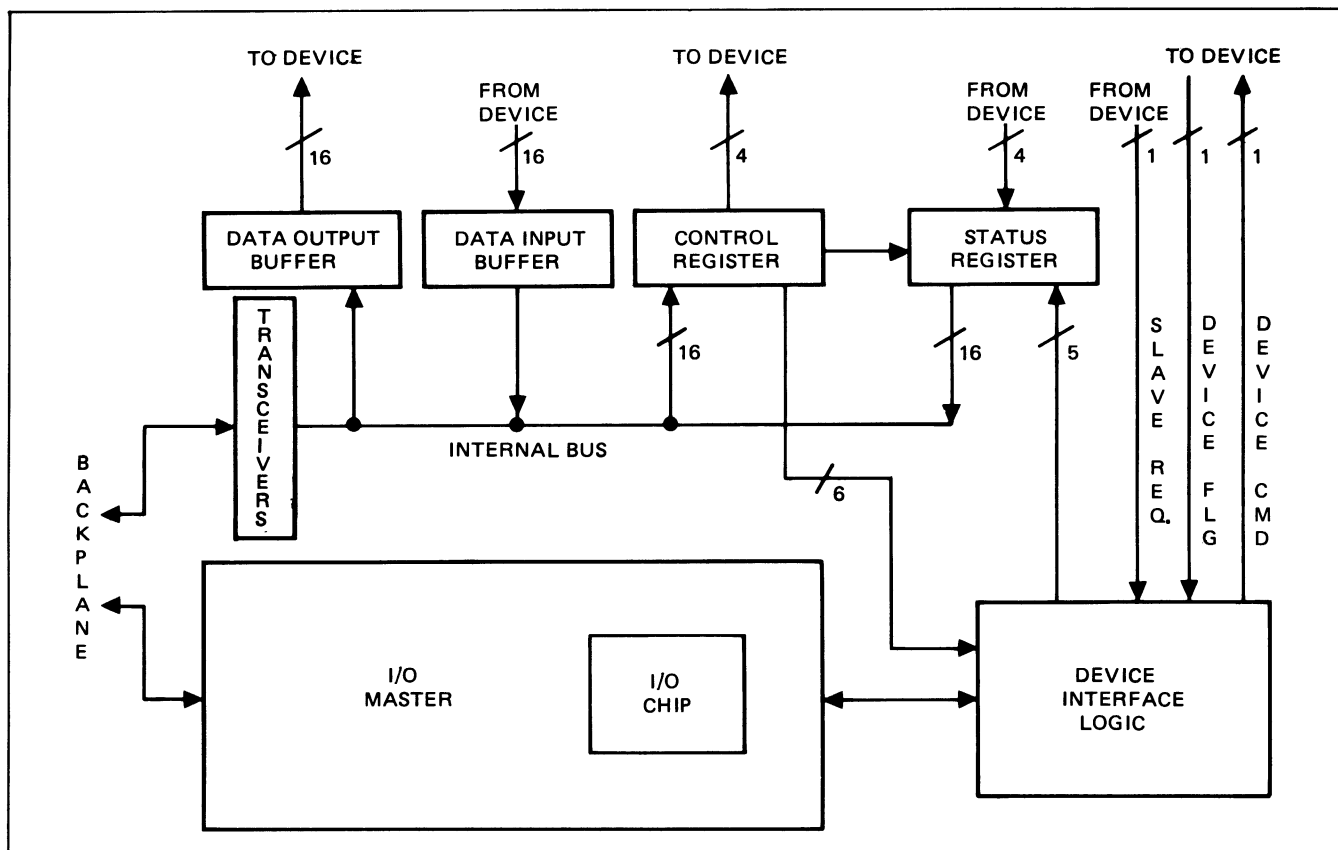
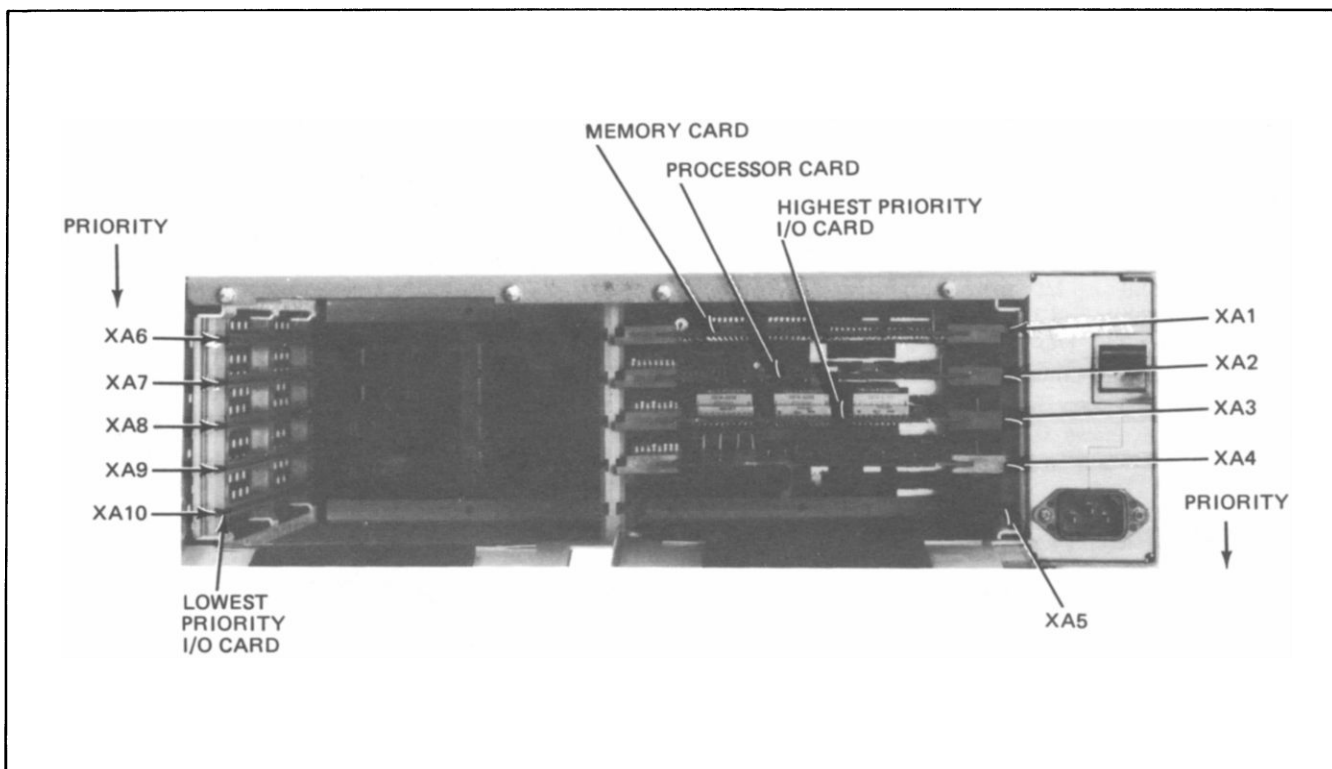


Figure 1-2. Parallel Interface Simplified Block Diagram



7700-480

Figure 1-3. Typical L-Series Card Cage Layout

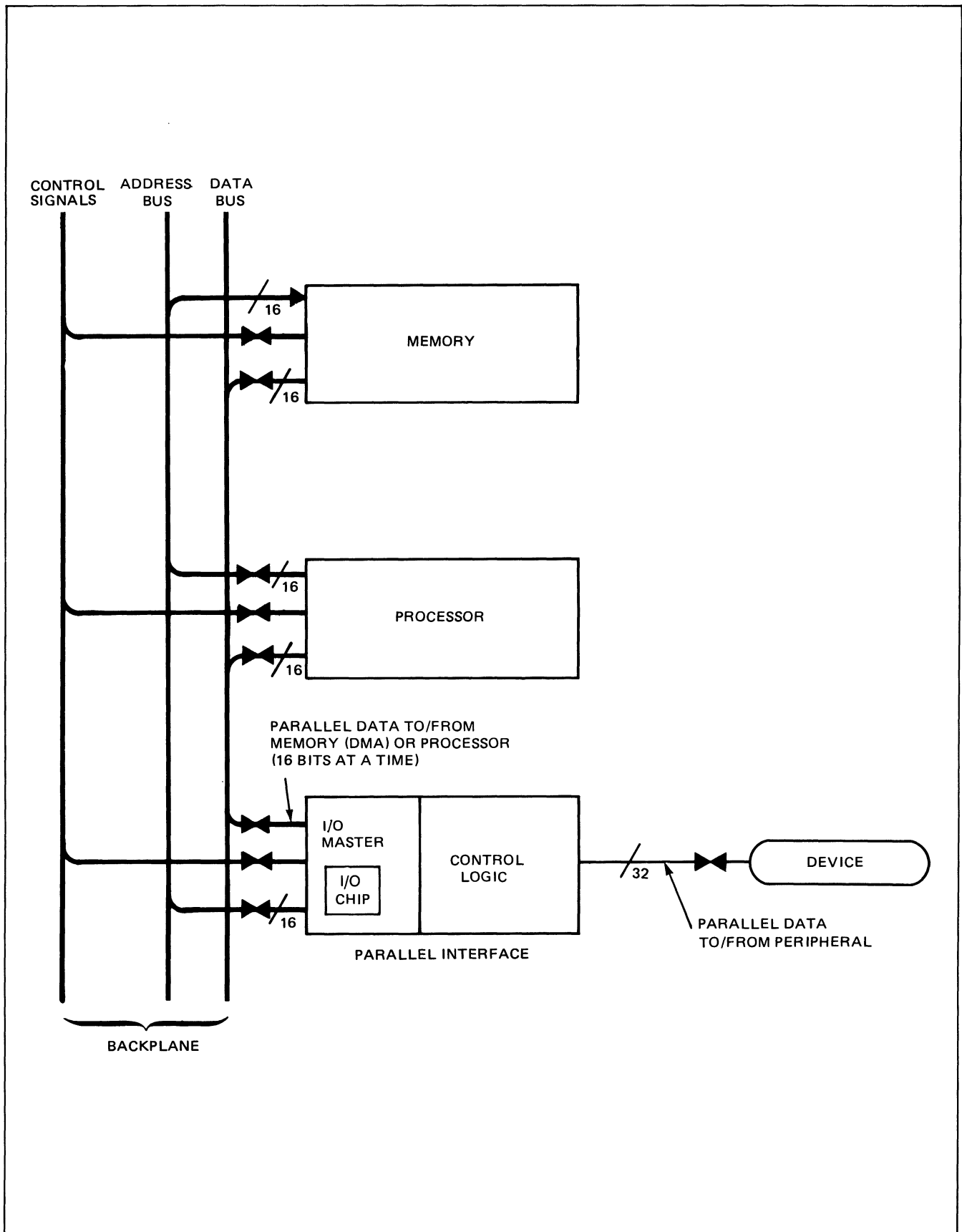


Figure 1-4. Parallel Interface in Typical System Environment

Table 1-1. Specifications

DATA TRANSFER CAPABILITIES

PROTOCOL: Transfers either 8 or 16 bits at a time in parallel.

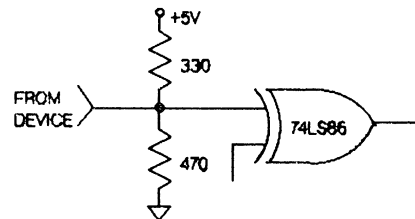
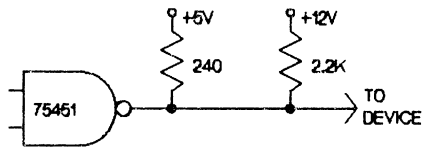
RATE:	CPU	A600	A700	A900
	INPUT (words/sec)	850k	790k	740k
	OUTPUT (words/sec)	730k	650k	500k
	CPU-CPU	typically less than 50% of output rate		

Conditions: Measured at the card edge in a quiescent RTE-A environment where the PIC was the highest priority interface. DVCMD- was inverted and wrapped around to produce DEVFLG. NOTE: k = one thousand.

DEVICE INTERFACE CHARACTERISTICS

+12V/+5V Device Interface: As delivered, the PIC is configured for +5V device interface. The +5V interface is best for high speed applications such as computer-to-computer communications. The +12V interface accommodates devices such as paper-tape readers and punches. Pull resistors R6, R7, R8, R9, R10, and R11 from their sockets to enable the +12V interface.

+5V Device Interface



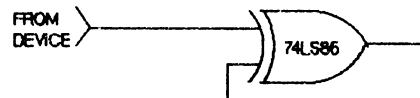
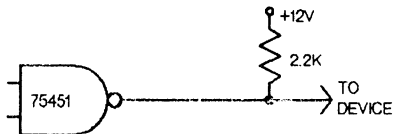
Device Command and Data Output

V_{OL} max = 0.7V
 V_{OH} max = 6.0V
 V_{OH} min = 4.0V
 I_{OL} max = 270mA (sink)
 I_{OH} max = 4mA (source)

Data Input

I_{IL} max = 16mA (source)
 I_{IH} max = 4mA (sink)
 V_{IL} max = 0.8V
 V_{IH} min = 2V
 V_{IH} max = 15V

+12V Device Interface



Device Command and Data Output

V_{OL} max = 0.7V
 V_{OH} max = 12.6V
 V_{OH} min = 8V
 I_{OL} max = 290mA (sink)
 I_{OH} max = 7.8mA (source)

Data Input

I_{IL} max = 0.8mA (source)
 I_{IH} max = 40μA
 V_{IL} max = 0.8V
 V_{IH} min = 2V
 V_{IH} max = 15V

Table 1-1. Specifications (continued)

8/16 Bit Interface: Many paper-tape readers and punches, and most line printers only transfer eight bits at a time. When interfacing to such 8-bit devices, the PIC may be programmed to byte-pack in hardware (see Section III of this manual).

Clocked/Transparent Mode: Most PIC applications utilize a device-flag/device-command handshake, which is the clocked mode.

In transparent latch mode no device-flag/device-command handshake is needed. An application where transparent mode can be used is sensing the state of up to 16 digital input lines connected to 16 different devices. Instead of being clocked, this information is dynamically available to the user. See Section IV for information on this type of operation.

PHYSICAL CHARACTERISTICS

Size:	17.15 by 28.91 cm (6.75 by 11.38 inches)
Backplane Interconnects:	Two 50-finger edge connectors which plug into two sockets (P1 and P2) mounted on the backplane.
Device Interconnects:	One 48-finger edge connector on which a cable hood (J1) may be connected.

POWER REQUIREMENTS

+5 Volt Device Interface				+12 Volt Device Interface			
Voltage	Current	Power	Dissipation	Voltage	Current	Power	Dissipation
+5V	1.94A	10.18W		+5V	1.61	8.43W	
+12V	179mA	<u>2.26W</u>		+12V	175mA	<u>2.21W</u>	
	Total	12.44W			Total	10.64W	

DEVICE INTERFACE

16 bits in (DATA)
 16 bits out (DATA)
 4 bits out (CONTROL or ADDRESS or COMMAND)
 4 bits in (STATUS)
 Device Flag
 Device Control

OPERATING TEMPERATURE RANGE

0 to 55° C

2-1. INTRODUCTION

This section provides information on unpacking, inspecting, installing, and checking the operation of the HP 12006A Parallel Interface.

2-2. UNPACKING AND INSPECTION

If the parallel interface is ordered with a computer, it is installed at the factory. When this is the case, it is necessary only to check the operation of the peripheral device and the parallel interface, after the computer and the peripheral device are installed. Checkout instructions are furnished in paragraph 2-15. If the parallel interface is ordered separately, inspect the carton containing the interface before opening it. If there is evidence of damage, if water stains are visible, or if the box rattles, request that the carrier's agent be present when the box is opened.

Inspect each part as it is unpacked. Look for such damage as cracks, dents, broken components, detached parts, corrosion, water damage, etc. If any part is damaged, retain the carton, packing material, and shipping papers, and immediately notify the carrier and the nearest Hewlett-Packard Sales and Service Office. The Sales and Service Office will arrange for repair or replacement of damaged parts without waiting for settlement of claims against the carrier. (HP Sales and Service Offices are listed at the back of this manual.)

After inspecting all components, refer to Section I, paragraph 1-11 to insure that no parts are missing. Also check the part numbers listed in paragraph 1-11 against the part numbers on the parts. If parts are missing, or if an incorrect component has been furnished, notify the nearest Hewlett-Packard Sales and Service Office.

2-3. PREPARATION FOR INSTALLATION

2-4. COMPUTATION OF CURRENT REQUIREMENTS

The circuit card obtains its operating voltages from the computer power supply, through the backplane. Before installing the card, it is necessary to determine whether the added current will overload the power supply. (If the circuit card was installed at the factory, the required calculations have been made, and it has been determined that an overload will not occur.) The current requirements of the parallel interface card are listed in Section I, table 1-1.

2-5. INTERFACE REQUIREMENTS

2-6. BACKPLANE TO PARALLEL INTERFACE

All interactions between the parallel interface and the central processor and memory cards occur on the backplane. The backplane interface is therefore the most complicated interface on the PIC. Connections from the backplane to the PIC are listed in table 2-1 (connector P1), and table 2-2 (connector P2).

2-7. CABLE RECOMMENDATIONS

When fabricating cables for the PIC, a shielded cable with twisted pairs is recommended. The shield should be connected to the spring clip provided with the 48-pin connector kit (this provides a connection to the computer chassis). The shield should not be connected at the other end of the cable. The ground wires from the twisted pairs should be connected to DC ground at both ends of the cable. At the PIC end, the ground can be connected to J1-24, BB.

2-8. INTERCONNECTING CABLE CONNECTIONS

The pin connections for the interconnecting cable used to connect the PIC to a peripheral device are contained in table 2-3. This table lists the signals at J1 and provides a place for recording your device wiring scheme.

2-9. COMPUTER-TO-COMPUTER COMMUNICATIONS

Computer-to-computer communications with the PIC can be accomplished with an interconnecting cable wired as shown in table 2-4. If twisted pairs are used, the ground wires should be connected to pins 24, BB, or signal ground, at each end. If the cable is shielded, the shield should be connected to chassis ground.

2-10. SWITCH SELECTABLE OPTIONS

The switch selectable options are the 6-bit select code (U1S3-U1S8) and the device command sense bit (U1S2). The switches are located near the cable connector (J1) on the PIC (see figure 1-1). The Virtual Control Panel (VCP) function is not implemented on the PIC.

Table 2-1. Backplane Connections, Connector P1

P1-	SIGNAL NAME	SIGNAL DEFINITION
1	ICHID-	Interrupt Chain In Disable
2	ICHOD-	Interrupt Chain Out Disable
3	MCHID-	Memory Chain In Disable
4	MCHOD-	Memory Chain Out Disable
5	MLOST-	Memory Lost
6	MCHODOC-	Memory Chain Out Disable Open Collector
7	PFW-	Power Fail Warning
8	SPARE 1	
9	SC0	Address Extension Bus Bit 0
10	SC1	Address Extension Bus Bit 1
11	SC2	Address Extension Bus Bit 2
12	SC3	Address Extension Bus Bit 3
13	GND	
14	GND	
15	SPARE 2	
16	GND	
17	SC4	Address Extension Bus Bit 4
18	SC5	Self Configure
19	AB0	Address Bus Bit 0
20	AB1	Address Bus Bit 1
21	AB2	Address Bus Bit 2
22	AB3	Address Bus Bit 3
23	AB4	Address Bus Bit 4
24	AB5	Address Bus Bit 5
25	AB6	Address Bus Bit 6
26	AB7	Address Bus Bit 7
27	AB8	Address Bus Bit 8
28	AB9	Address Bus Bit 9
29	AB10	Address Bus Bit 10
30	AB11	Address Bus Bit 11
31	AB12	Address Bus Bit 12
32	AB13	Address Bus Bit 13
33	AB14	Address Bus Bit 14
34	WE-	Write Enable
35	DB0	Data Bus Bit 0
36	DB1	Data Bus Bit 1
37	DB2	Data Bus Bit 2
38	DB3	Data Bus Bit 3
39	DB4	Data Bus Bit 4
40	DB5	Data Bus Bit 5
41	DB6	Data Bus Bit 6
42	DB7	Data Bus Bit 7
43	DB8	Data Bus Bit 8
44	DB9	Data Bus Bit 9
45	DB10	Data Bus Bit 10
46	DB11	Data Bus Bit 11
47	DB12	Data Bus Bit 12
48	DB13	Data Bus Bit 13
49	DB14	Data Bus Bit 14
50	DB15	Data Bus Bit 15

Table 2-2. Backplane Connections, Connector P2

P2-	SIGNAL NAME	SIGNAL DEFINITION
1	CPUTURN-	Processor Turn
2	GND	
3	REMEM-	Remote Memory
4	VALID-	Data Valid
5	IORQ-	I/O Handshake Request
6	INTRQ-	Interrupt Request
7	MP	Memory Protect
8	RNI-	Read Next Instruction
9	MEMGO-	Memory Cycle Initiation
10	PE-	Parity Error
11	SCHID-	Slave Chain In Disable
12	SCHOD-	Slave Chain Out Disable
13	IAK-	Interrupt Acknowledge
14	IOGO-	I/O Handshake Request Acknowledge
15	GND	
16	SLAVE-	Slave Request
17	GND	
18	MRQ-	Memory Request
19	GND	
20	FCLK-	Fast Clock
21	GND	
22	CCLK-	Communications Clock
23	PINT-	Priority Interrupt
24	SCLK-	System Clock
25	CRS-	Control Reset
26	PON	Power On
27	GND	
28	BUSY-	Memory Busy
29	GND	
30	GND	
31	GND	
32	GND	
33	GND	
34	GND	
35	+5V	
36	+5V	
37	+5V	
38	+5V	
39	+12M	
40	-12M	
41	+12V	
42	+12V	
43	-12V	
44	-12V	
45	+5M	
46	+5M	
47	AC 2	
48	AC 2	
49	AC 1	
50	AC 1	

Table 2-3. Cable Wiring List and J1 Signals

CONNECTOR B		CONNECTOR A		J1	SIGNAL NAME	DEFINITION
PIN	WIRE COLOR(s)	PIN				
---	---	---		1	IN0	Data from device
---	---	---		2	IN1	
---	---	---		3	IN2	
---	---	---		4	IN3	
---	---	---		5	IN4	
---	---	---		6	IN5	
---	---	---		7	IN6	
---	---	---		8	IN7	
---	---	---		9	IN8	
---	---	---		10	IN9	
---	---	---		11	IN10	
---	---	---		12	IN11	
---	---	---		13	IN12	
---	---	---		14	IN13	
---	---	---		15	IN14	
---	---	---		16	IN15	
---	---	---		17	ST0	Status from device (lsb)
---	---	---		18	ST1	Status from device (msb)
---	---	---		19	ST2	
---	---	---		20	ST3	
---	---	---		21	SLRQ	Slave Request
---	---	---		22	+5V	Device flag (Service Request)
---	---	---		23	SRQ	
---	---	---		24	GND	Data to device
---	---	---		A	OUT0	
---	---	---		B	OUT1	
---	---	---		C	OUT2	
---	---	---		D	OUT3	
---	---	---		E	OUT4	
---	---	---		F	OUT5	
---	---	---		H	OUT6	
---	---	---		I	OUT7	
---	---	---		K	OUT8	
---	---	---		L	OUT9	
---	---	---		M	OUT10	
---	---	---		N	OUT11	
---	---	---		P	OUT12	
---	---	---		R	OUT13	
---	---	---		S	OUT14	
---	---	---		T	OUT15	
---	---	---		U	CNT0	Control to device (lsb)
---	---	---		V	CNT1	
---	---	---		W	CNT2	
---	---	---		X	CNT3	Control to device (msb)
---	---	---		Y	SPARE	
---	---	---		Z	DVCMD	Device Command
---	---	---		AA	DVCMD	Device Command
---	---	---		BB	GND	

Table 2-4. Computer-to-Computer Cable Wiring List

CONNECTOR A		WIRE COLOR(s)	CONNECTOR B	
NOTES	PIN		PIN	NOTES
-----	1	-----	A	-----
-----	2	-----	B	-----
-----	3	-----	C	-----
-----	4	-----	D	-----
-----	5	-----	E	-----
-----	6	-----	F	-----
-----	7	-----	H	-----
-----	8	-----	J	-----
-----	9	-----	K	-----
-----	10	-----	L	-----
-----	11	-----	M	-----
-----	12	-----	N	-----
-----	13	-----	P	-----
-----	14	-----	R	-----
-----	15	-----	S	-----
-----	16	-----	T	-----
-----	17	-----	U	-----
-----	18	-----	V	-----
-----	19	-----	W	-----
-----	20	-----	X	-----
-----	A	-----	1	-----
-----	B	-----	2	-----
-----	C	-----	3	-----
-----	D	-----	4	-----
-----	E	-----	5	-----
-----	F	-----	6	-----
-----	H	-----	7	-----
-----	J	-----	8	-----
-----	K	-----	9	-----
-----	L	-----	10	-----
-----	M	-----	11	-----
-----	N	-----	12	-----
-----	P	-----	13	-----
-----	R	-----	14	-----
-----	S	-----	15	-----
-----	T	-----	16	-----
-----	U	-----	17	-----
-----	V	-----	18	-----
-----	W	-----	19	-----
-----	X	-----	20	-----
-----	23	-----	Z	-----
-----	24, BB	-----	24, BB	-----
-----	Z	-----	23	-----
-----		-----		-----
-----		-----		-----

2-11. VIRTUAL CONTROL PANEL INTERFACE SELECTION

Switch U1S1 must remain in the open (up) position. The Virtual Control Panel (VCP) function is not implemented on the PIC.

U1S1 open: The PIC will not operate as a VCP interface. Transitions of Slave Request will be ignored.

U1S1 closed: This position is not to be used.

2-12. DEVICE COMMAND SENSE SELECTION

Switch S2 is used to set the device command sense to a high true or low true Device Command (DVCMD).

S2 open: Active high Device Command (high true)

S3 closed: Active low Device Command (low true)

2-13. SELECT CODE SELECTION

Switches S3 through S8 determine the select code for the PIC.

Open switch: Logic one.

Closed switch: Logic zero.

S8 represents the least significant bit.

2-14. INSTALLATION

After insuring that the computer power supply can handle the added load, perform the following:

CAUTION

STATIC SENSITIVE DEVICE. Use Anti-static handling procedures (see page iii) when handling the interface.

- a. Set switch S1 open or closed depending on whether the PIC has been selected to operate as interface to a Virtual Control Panel (see paragraph 2-11).
- b. Set the Device Command (DVCMD) sense to high true or low true with switch S2 (see paragraph 2-12).
- c. Set the select code for the PIC with switches S3 through S8 (see paragraph 2-13).
- d. Turn off power at the computer and the I/O device. Install the PIC in the desired slot in the computer card cage. Components on the card must be on the same side of the card as for other cards in the I/O slots.

When installing the card, use care not to damage components or traces on the card or on adjacent cards. Press the card firmly into place.

- e. Connect the appropriate cable from the I/O device to the end of the PIC.

2-15. CHECKOUT

To verify operation of the parallel interface card, see Section V, paragraph 5-3, steps 1, 2, and 3.

2-16. RESHIPMENT

If an item of the kit is to be shipped to the nearest Hewlett-Packard Sales and Service Office for repair, attach a tag to the item identifying the owner and indicating the service to be performed. Include the product number.

Pack the item in the original factory packing material. If the original material is not available, good commercial packing material should be used. Reliable commercial packing and shipping companies have the facilities and materials to adequately repack the item.

3-1. INTRODUCTION

This section provides assembly-language programming procedures for the parallel interface card (PIC) and its peripheral device. For information on assembly-language programming, refer to the HP 1000 L-Series Reference Manual, part no. 02103-90007. In addition, A-Series users should refer to the HP 1000 A600/A700 DDL Programming Reference Manual, part no. 24612-90002.

The PIC has many capabilities such as byte packing, handling its own Direct Memory Access (DMA), and decoding its own instructions from the central processor unit (CPU).

There are two approaches to be taken when programming the parallel interface card:

1. Programmed I/O. Simple input and output subroutine examples are shown in figure 3-1.
2. Direct Memory Access (DMA), which offers the advantage of very low central processor overhead.

SAMPLE OUTPUT SUBROUTINE		
OPCODE	OPERAND	COMMENTS
SFS	PIC	DEVICE BUSY?
JMP	*-1	YES, WAIT
OTA	PIC	NO, OUTPUT DATA
STC	PIC	ENABLE DEVICE

SAMPLE INPUT SUBROUTINE		
OPCODE	OPERAND	COMMENTS
STC	PIC	ENABLE DEVICE
SFS	PIC	DEVICE BUSY?
JMP	*-1	YES, WAIT
LIA	PIC	NO, READ NEW DATA

Figure 3-1. Sample I/O Subroutines

3-2. USE OF THE GLOBAL REGISTER

Every I/O interface card (parallel interface, serial interface, etc.) in the HP 1000 L/A-Series Computer System contains a global register. The global register is located in the I/O chip and is a six-bit register which contains a select code. See figure 3-2 for a block diagram of the I/O chip.

All global registers on all interface cards are controlled by the CPU, thus all global registers contain the same select code. The global register may be loaded with an OTA 2 or OTB 2 I/O instruction, enabled with a CLF 2 I/O instruction and disabled with an STF 2 I/O instruction. When the global register is enabled, any I/O instruction which is executed by the CPU automatically applies to the card whose select code is in the global register. For the PIC, for example, if the global register contains the PIC's select code, the current I/O instruction is decoded and executed by the PIC. Using the global register to store select code frees the six least significant bits of I/O instructions (these bits do not need to store the select code of the I/O device which is to receive the I/O instruction). Thus, these six bits can be used to address a register on I/O interface cards. On the parallel interface card, there are six such registers: one for data, one for control, one for status, and three for DMA control.

Data may be transferred to and from the PIC with or without the global register enabled. To access the PIC's control and status registers, however, the global register must be used.

3-3. I/O INSTRUCTION SET

The I/O master executes twelve I/O instructions as follows:

CLC Clear Control
 CLF Clear Flag
 LIA Load Into A
 LIB Load Into B
 MIA Merge Into A
 MIB Merge Into B
 OTA Output A
 OTB Output B
 SFC Skip if Flag Clear
 SFS Skip if Flag Set
 STF Set Flag
 STC Set Control

The six bit global register allows a maximum of 64 (decimal) select codes. The I/O master, however, executes only a portion of this maximum. Select codes 00 through 17 (octal) are reserved for the central processor, leaving 20 through 77 (octal) available for the I/O system.

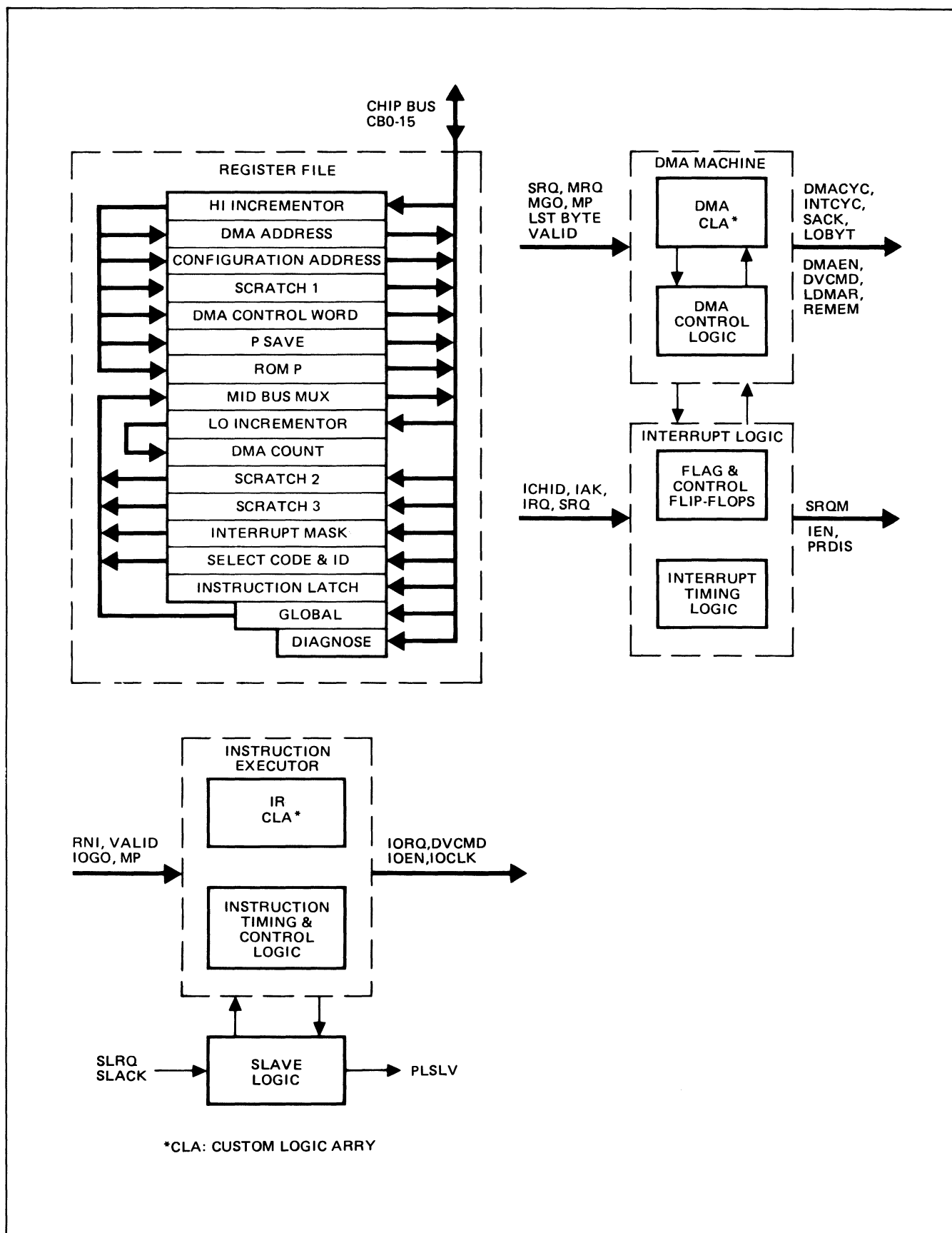


Figure 3-2. I/O Chip Block Diagram

3-4. INSTRUCTION USAGE SUMMARY

Table 3-1 lists all the instructions recognized by the I/O Chip by their select code. There are three conditions relevant to the instruction execution. These conditions are as follows:

- Is the global register (GR) enabled?
- Do the contents of the GR equal the I/O chip's select code, (GR = SC)?
- Do the lower six bits of the instruction equal the I/O chip's select code, (IR = SC)?

The summary indicates which conditions must be met for instruction execution by listing Y for yes, N for no, and X for don't care in each column.

3-5. OUTPUT CONTROL WORDS

Five control words can be received by the PIC. These control words are loaded into five registers. Four of these registers (registers 20,21,22 and 23) are located in the I/O chip and are used only in the DMA mode. These registers are described in paragraphs 3-11 through 3-13.

One of the control words is used in any mode (DMA or non-DMA) and is the only control word necessary when DMA is not used. This control word is loaded into register 31 (U44, U84), and may be sent to the PIC using an OTA 31 or OTB 31 only when the global register is enabled.

3-6. CONTROL REGISTER 31

Register 31 control word is used for both DMA and programmed I/O. Its contents usually depend on the type of device being used.

Two control word examples are as follows:

HP 2895 Paper Tape Punch

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	1	0	0	0	0	0	1	1	0	0	0	0

HP 2748 Paper Tape Reader

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	1	0	0	0	0	0	0	1	1	0	0	0	0

The definitions of the bits in register 31 are as follows:

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TSTU	SPARE	DFS	DCL	PLV	LBV	IRQ	TSTL	SRM	DRM	SNS	CTL3	CTL2	CTL1	CTL0	

Bits 0 - 3: CTL0 through CTL3

Four general purpose lines that may be used to address, control, or handshake with various types of peripheral devices. These lines are latched onto the PIC during execution of an OTA 31 (global register enabled) and during DMA self-configuration, and constantly driven out to the peripheral device.

Bit 4: SNS Sense Select Signal

0 = Inverts all 40 status, data, and control signals transferred between the PIC and the device (16 output data lines, 16 input data lines, four control lines to the device, and four status lines from the device). Therefore, this bit, if clear, causes a low true (ground) device interface.

1 = All 40 signals are not inverted, and a high true (positive) device interface exists.

Bit 5: DRM Data Register Mode

1 = Causes data register 30 (input data register, U53 and U83) to be loaded on each DEVICE FLAG signal assertion.

0 = Causes data register 30 to act as a transparent latch so that 16 bits of data are dynamically available.

Bit 6: SRM Status Register Mode

1 = Causes status register 32 (U54, U64) to be loaded on each Device Flag assertion.

0 = Causes status register 32 to act as a transparent latch so that the status is dynamically available.

Bit 7: TSTL Test Lower Bytes

Used by diagnostics to test the operation of the lower bytes of the control and status registers.

Bit 8: IRQEN Interrupt Request Enable

1 = Enables the assertion of ST0 to set the Interrupt Request (IRQ) line, thereby causing Flag 30.

0 = Disables Interrupt Request from being asserted.

Bit 9: LBYEN Last Byte Enable

LBYEN enables early termination of a DMA input transfer.

1 = Enables the assertion of ST1 to cause orderly shut-down of a DMA transfer before word count rollover occurs.

0 = Prevents assertion of LSBYT (last byte), DMA continues until word count rollover occurs.

When this feature is used, ST1 should be asserted prior to the Device Flag accompanying the last word or byte. The assertion of ST1 will not be recognized until the Device Flag Signal is also asserted.

Table 3-1. I/O Chip Instructions By Select Code

INSTRUCTION	FUNCTION	GR ON	GR =SC	IR =SC	NOTES
LI* 0	Read interrupt mask	X	Y	X	
MI* 0	Merge interrupt mask	X	Y	X	
OT* 0	Write interrupt mask	X	X	X	
CLF 2	Enable GR	X	X	X	
STF 2	Disable GR	X	X	X	
LI* 2 [,C]	Read GR	X	Y	X	1, 9
MI* 2 [,C]	Merge GR	X	Y	X	1, 9
OT* 2 [,C]	Write GR	X	X	X	
STC 2 [,C]	Enable Slave logic	X	X	X	1, 2
	Enable GR				
CLC 3	"BREAK" to front panel	X	X	X	2
HLT XX	"BREAK" to front panel	X	X	X	2
LI* 3	Read P SAVE	X	X	X	2
MI* 3	Merge P SAVE	X	X	X	2
OT* 3	Write P SAVE	X	X	X	2
LI* 3,C	Read ROM P	X	X	X	2
MI* 3,C	Merge ROM P	X	X	X	2
OT* 3,C	Write ROM P	X	X	X	2
SFC 20	Skip if FLG 20 clear	Y	Y	X	3
SFS 20	Skip if FLG 20 set	Y	Y	X	
CLF 20	Clear FLG 20 and FLG 21	Y	Y	X	
STF 20	Set FLG 20	Y	Y	X	
STC 20 [,C]	Enable DMA self configuration	Y	Y	X	
CLC 20 [,C]	Disable DMA self configuration	Y	Y	X	
LI* 20 [,C]	Read DMA configuration address	Y	Y	X	
MI* 20 [,C]	Merge DMA configuration address	Y	Y	X	
OT* 20 [,C]	Write DMA configuration address	Y	Y	X	
	Clear FLG 20 and FLG 21				
SFC 21	Skip if FLG 21 clear	Y	Y	X	4
SFS 21	Skip if FLG 21 set	Y	Y	X	
CLF 21	Clear FLG 21	Y	Y	X	
STF 21	Set FLG 21	Y	Y	X	
STC 21 [,C]	Enable DMA transfers	Y	Y	X	
CLC 21 [,C]	Disable DMA transfers	Y	Y	X	
LI* 21 [,C]	Read DMA Control word	Y	Y	X	
MI* 21 [,C]	Merge DMA Control word	Y	Y	X	
OT* 21 [,C]	Write DMA Control word	Y	Y	X	
	Clear FLG 21				
SFC 22	Skip if FLG 22 clear	Y	Y	X	5
SFS 22	Skip if FLG 22 set	Y	Y	X	
CLF 22	Clear FLG 22	Y	Y	X	
STF 22	Set FLG 22	Y	Y	X	
CLC 22 [,C]	Force DMA reconfiguration	Y	Y	X	
LI* 22 [,C]	Read DMA address	Y	Y	X	
MI* 22 [,C]	Merge DMA address	Y	Y	X	
OT* 22 [,C]	Write DMA address	Y	Y	X	
	Clear FLG 22				
SFC 23	Skip if FLG 20, FLG 21, AND FLG 22 ALL Clear	Y	Y	X	6
SFS 23	Skip if FLG 20 OR FLG 21 OR FLG 22 Set (inclusive OR)	Y	Y	X	
CLF 23	Clear FLG 20, FLG 21, and FLG 22	Y	Y	X	
CLC 23 [,C]	Terminate DMA operation	Y	Y	X	
LI* 23 [,C]	Read DMA Count	Y	Y	X	
MI* 23 [,C]	Merge DMA Count	Y	Y	X	
OT* 23 [,C]	Write DMA Count	Y	Y	X	
	Clear FLG 20, FLG 21, and FLG 22				

Table 3-1. I/O Chip Instructions By Select Code (Continued)

INSTRUCTION	FUNCTION	GR ON	GR =SC	IR =SC	NOTES
SFC 24	Skip if DMA disabled (DMAEN — asserted)	Y	Y	X	
SFS 24	Skip if DMA enabled (DMAEN — not asserted)	Y	Y	X	
LI* 24	Read Scratch 1	Y	Y	X	
MI* 24	Merge Scratch 1	Y	Y	X	
OT* 24	Write Scratch 1	Y	Y	X	
LI* 25	Read Scratch 2	Y	Y	X	
MI* 25	Merge Scratch 2	Y	Y	X	
OT* 25	Write Scratch 2				
LI* 26	Read Scratch 3	Y	Y	X	
MI* 26	Merge Scratch 3	Y	Y	X	
OT* 26	Write Scratch 3	Y	Y	X	
SFC 30	Skip if FLG 30 clear	Y	Y	X	7
SFS 30	Skip if FLG 30 set	Y	Y	X	
CLF 30	Clear FLG 30	Y	Y	X	
STF 30	Set FLG 30	Y	Y	X	
STC 30 [,C]	Set CNTRL 30 and issue DVCMD	Y	Y	X	
CLC 30 [,C]	Clear CNTRL 30	Y	Y	X	
LI* 30 [,C]	Read device data	Y	Y	X	
MI* 30 [,C]	Merge device data	Y	Y	X	
OT* 30 [,C]	Write device data	Y	Y	X	
	Clear FLG 30				
OT* 31	Write interface control word	Y	Y	X	
LI* 32	Read interface status	Y	Y	X	8
MI* 32	Merge interface status	Y	Y	X	
OT* 32	Reset interface status	Y	Y	X	9
SFC SC	Skip if FLG 30 clear	N	X	Y	7
SFS SC	Skip if FLG 30 set	N	X	Y	
CLF SC	Clear FLG 30	N	X	Y	
STF SC	Set FLG 30	N	X	Y	
STC SC [,C]	Set CNTRL 30 and issue DVCMD	N	X	Y	
CLC SC [,C]	Clear CNTRL 30	N	X	Y	8
LI* SC [,C]	Read device data	N	X	Y	10
MI* SC [,C]	Merge device data	N	X	Y	10
OT* SC [,C]	Write device data	N	X	Y	
	Clear FLG 30				

SC = Interface select code

Notes:

- The [,C] is always executed even if the primary instruction is not.
- The SLAVE logic must be enabled; i.e., SLRQ LOW at power up.
- FLG 20 is set by DMA upon completion of self configured DMA block transfer which is not to be followed by another self configuration.
- FLG 21 is set by DMA upon completion of any block transfer which is not to be followed by a self configuration.
- FLG 22 is set by DMA if a parity error occurs during a DMA read.
- FLG 23 is the logical OR of flags 20 through 22.
- FLG 30 and CNTRL 30 are controlled by the Flag and Control flip-flops located in the I/O chip.
- The I/O chip indicates only that the select code is in the range 32 to 77, it is up to the user to decode any specific select code.
- Serial I/O cards, by convention, use this instruction as a card reset.
- When the I/O chip is in diagnose mode, these instructions fetch the following:
 - Diagnose mode 1 — the interface's select code and ID word.
 - Diagnose mode 2 — the global register and I/O chip status bits.

Bit 10: PLV Pulse Level

PLV selects between a pulsed or a level Device Command signal.

- 1 = Produces a Device Command signal, which is a pulse with a duration of one period of SCLK, or approximately 227 nsec.
- 0 = Produces a level mode Device Command.

The Device Command is asserted upon execution of a STC, or automatically during each DMA transfer. The level mode Device Command is deasserted on a selected edge of Device Flag. Also, while DMA is not running, the level mode Device Command signal may be deasserted by clearing the Control flip-flop (executing a CLC 30).

Bit 11: DCL Device Command Clear

DCL selects which edge of Device Flag clears Device Command. This bit only has effect if bit 10 above is clear.

- 1 = Device Command will be cleared on the opposite edge of Device Flag than that which caused the SRQ.
- 0 = Device Command will be cleared on the same edge of Device Flag which caused the assertion of SRQ.

Bit 12: DFS Device Flag Select

DFS selects which edge of Device Flag causes the Service Request (SRQ) signal.

- 1 = Positive-going edge of Device Flag causes SRQ.
- 0 = Negative-going edge of Device Flag causes SRQ.

Bits 13 and 14: Not used (spare).

Bit 15: TSTU Test Upper Bytes

Used by diagnostics to check the operation of the upper bytes of the control and status registers.

3-7. INPUT STATUS WORD, REGISTER 32

It is often desirable to interrogate a device as to its status in order to obtain such information as the cause of an interrupt or the state of a control circuit. Sixteen bits of status information are available in a software-accessible status word, which may be fetched using an LIA 32 or LIB 32 with the global register enabled.

Definitions of the bits in status register 32 (U54, U64) are as follows:

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TS	SLV	DMA	PACK	CN	CN	CN	CN	TS	OFF	FL	DC	ST3	ST2	ST1	ST0
TU		ON-		T3	T2	T1	T0	TL		AG	SS				

Bits 0 - 3: ST0 - ST3 Status 0 - 3

These four bits provide the PIC with status information from the device to which it is connected. These bits can be

latched into register 32 on each Device Flag assertion or they can be dynamically available, according to the sense of bit 6 of register 31 (see paragraph 3-6).

Bit 4: DCSS Device Command Sense Switch

DCSS indicates the setting of the Device Command Sense Switch.

- 1 = Active high (high true) Device Command (DVCMD) was selected.
- 0 = Active low (low true) Device Command (DVCMD) was selected.

Bit 5: FLAG

FLAG reads the logical sense of the Device Flag line. Initially, FLAG should be zero. This information is most often used for diagnostic purposes.

Bit 6: DFF Device Command Flip-Flop

DFF reads the sense of the Device Command flip-flop. This bit is most often used for diagnostic purposes.

Bit 7: TSTL Test Lower Byte

TSTL is used by diagnostics to check the operation of the lower byte of the control (register 31) and status (register 32) registers.

Bits 8 - 11: CNT0 - CNT3

These four bits check the status of general purpose lines CNT0 through CNT3 of control register 31. CNT0 through CNT3 of control register 31 are used for address, control, or handshake with various types of peripheral devices.

Bit 12: PACK Pack Bytes

PACK is the Q output of the PACK flip-flop.

- 1 = DMA is executing in byte mode, with two bytes packed into each word.
- 0 = Either DMA is executing in word mode, or DMA is not currently running.

Bit 13: DMAON- DMA On

DMAON- is the Q- output of the DMAON flip-flop.

- 0 = DMA is executing.
- 1 = DMA is not executing.

Bit 14: SLV Slave

0 = PIC is in normal mode of operation.

- 1 = PIC is requesting slave mode (access to the Virtual Control Panel code).

Bit 15: TSTU Test Upper Byte

TSTU is used by diagnostics to check the operation of the upper byte of the control (register 31) and status (register 32) registers.

3-8. DIRECT MEMORY ACCESS (DMA) OPERATION

The PIC is capable of transferring data directly to or from memory (direct memory access). All control logic and registers necessary to supervise the memory transaction are contained in the I/O chip. Appropriate signals are available to the interface logic to signal when to enable its data onto the system data bus, when to receive data from the system data bus, and when to initiate the next interface operation. In addition, signals to the I/O chip indicate when a data transfer is needed and when an interrupt-requesting condition has occurred.

Any given card has a maximum DMA rate at which it is capable of running. In order to achieve this maximum rate however, there can be no other requests on the backplane. Typically, there are other transactions on the backplane which degrade the maximum possible DMA rate. When the processor decides to fetch an instruction at the same time as an interface card is preparing for DMA, that DMA cycle can be held off for 908 ns. If an interface card is in the highest priority slot, it can be held off by the processor, or, in addition by a lower priority card doing DMA for a worst case of 454 ns per transfer. All DMA rate specifications given in Table 1-1 assume the card in question is plugged into the highest priority slot. When plugged into a lower priority slot, DMA rates can not be guaranteed when the additive rates of the higher priority cards are capable of consuming the total backplane bandwidth (2.72 Mbytes). Typically, however, even in a busy system, the backplane is only fully congested for very short periods of time, so that even the lowest priority I/O cards transfer at rates very close to their nominal specifications.

3-9. DMA CONTROL AND STATUS WORDS

Software DMA set-up and control involves five different control and status words, each of which is associated with a different register. Four of these status and control registers are located in the I/O chip. Their numbers and functions are listed below:

DMA Register Number 20, DMA Self-Configuration Register, In or Out

DMA Register Number 21, DMA Control Register, In or Out

DMA Register Number 22, DMA Address Register, In or Out

DMA Register Number 23, Word/Byte Count Register, In or Out

3-10. DMA SELF-CONFIGURATION, REGISTER 20

The DMA self-configuration register contains the address of the DMA triplets or quadruplets. A DMA triplet is of the form control bits, transfer address, and word/byte count. The triplet words are the words to be used in regis-

ters 21, 22, and 23, respectively. A DMA quadruplet is of the form control bits, interface control, transfer address, and word byte count, to be put in registers 21, 31, 22, and 23, respectively.

3-11. DMA CONTROL WORD 1, REGISTER 21

The bit definitions for DMA control word 1 are as follows:

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CONT	DV CMD	BYTE	RES	CINT	REM	FOUR	AUTO	IN	SPARE	RESERVED					

Bits 0 - 4: Reserved for expanded memory.

Bits 5 & 6: Not used.

Bit 7: IN

1 = Indicates that the direction of data transfers is FROM the PIC, TO the memory.

0 = Indicates that the direction of data transfers is FROM the memory, TO the PIC.

Bit 8: AUTO

AUTO has different meanings depending on whether bit 7, above, is set.

Meaning on Output:

1 = DMA control logic automatically performs the first data transfer once DMA is configured to output.

0 = Once a DMA output is configured, the DMA control logic waits for the PIC to assert SRQ- (Service Request) before performing the first data transfer.

Meaning on Input:

1 = Last input transfer will be followed by a DVCMD pulse.

0 = The last DVCMD pulse will be suppressed.

More specifically, AUTO will always be set on output. On input, AUTO will be clear for a device such as a tape reader, but for computer-to-computer communications, AUTO must be set on input in order for the DMA in the remote computer to terminate.

Bit 9: FOUR

1 = Indicates that there are four words to be fetched for the current DMA configuration.

0 = Indicates that there are three DMA control words to be fetched for the current DMA configuration.

Bit 10: REM Remote Memory

1 = All memory requests will be accompanied by the REMEM (Remote Memory) signal, which disables standard memory and enables remote memory.

0 = Remote memory is not enabled.

Bit 11: CINT Completion Interrupts

- 1 = Inhibits DMA transfer completion interrupts.
- 0 = Interrupt is to be requested by the DMA logic when the word/byte count rolls over (goes from -1 to 0).

Bit 12: RES Residue

- 1 = If set, and if DMA is enabled to self-configure, i.e., a STC 20 has been executed, DMA will write its word/byte count residue into the location from which it read the word/byte count.
- 0 = Word/byte count residue is not written.

Bit 13: BYTE

- 1 = Indicates that the DMA transfer is to be conducted in byte mode, i.e., each data transfer is counted as one byte. Byte mode transfers are packed, two bytes per word, with the left byte (bits 15 - 9 of the data word) being transferred first.
- 0 = Each data transfer will be a full 16-bit word.

Bit 14: DVCMD Device Command

- 1 = DMA control logic will issue a Device Command (DVCMD) signal immediately following each data transfer from the interface logic. (After each word in word mode (see bit 13), after each byte in byte mode.)
- 0 = Device Command is not issued.

Note that normal operation of the PIC requires that this bit always be set.

Bit 15: CONT Continue

- 1 = If set, and an STC 20 has been executed, then at the end of a DMA transfer the I/O chip will fetch the next set of DMA control words and reconfigure itself to start a new transfer.
- 0 = DMA will stop at the end of the current transfer.

3-12. DMA ADDRESS, REGISTER 22

DMA control word 2 is the 15-bit (bits 0 - 14) address of the next memory location to be accessed by DMA. The most significant bit (bit 15) cannot be controlled by OTA 22 or OTB 22 and will be the complement of control word 1, bit 7 (IN) when fetched by an LIA 22.

3-13. DMA WORD/BYTE COUNT, REGISTER 23

The word/byte count register, register number 23, is a 16-bit register whose value is the twos complement of the number of data elements to transfer. A data element may be either a word or a byte, as indicated by bit 13 of the DMA control word (contained in register number 21).

The end of a data transfer is indicated by the transition of the word/byte count register's value from -1 to 0. (Rollover from octal 177777 to 000000 occurs.) This allows up

to 65,536 data elements to be transferred at any one time. The memory size (32,768 words maximum) limits a word transfer to a length of 32,768. The hardware does not detect this, however, so it is the responsibility of the programmer not to exceed this limit.

3-14. DMA TRANSFER OPERATION

A DMA transfer is started by configuring the DMA control register, DMA address register, word/byte count register and the output control word (described in paragraph 3-6), and then issuing an STC instruction to register number 21 (DMA control register).

3-15. DMA INPUT TRANSFER. An input transfer is defined as being from the peripheral device to memory. If the transfer is in word mode, a Device Command (DVCMD) signal and a memory access are generated immediately. If the transfer is in byte mode, the DMA control logic merely responds to the PIC with DVCMD and changes the sense of its byte indicator line (which indicates to the PIC which of the two bytes/word is involved in the transfer). When the second byte transfer is requested, the memory write request is generated. The memory request goes directly to the backplane where memory access priority is determined by the location of the requesting card in respect to the processor (the closer a card is to the processor, the higher the priority). When the memory access request is granted, the data is transferred, the DMA word/byte count and DMA address registers are incremented, and the DMA control logic is ready to accept another data transfer request from the interface logic.

3-16. DMA OUTPUT TRANSFER. A DMA output transfer is defined as being from memory to the parallel interface card. For an output transfer, a memory access request is generated immediately. As soon as the data is available from memory, it is passed to the PIC. The data is followed by a Device Command (DVCMD) signal.

3-17. DMA TRANSFER TERMINATION. A DMA data transfer continues as described in paragraphs 3-16 and 3-17 above until a terminating condition is detected. The terminating conditions are:

- a. Word count transition from -1 to 0. (Rollover from octal 177777 to 000000 occurs.) This indicates that all the data elements that were requested to be transferred have been transferred.
- b. Detection of a Control Reset (CRS) signal. This signal is generated by the central processor during its power-up sequencing, or by execution of a CLC 0 instruction.
- c. Parity error indication from memory.
- d. Assertion of LSBYT.

Note that the PIC will effectively suspend a DMA transfer operation if the peripheral device does not assert Device Flag.

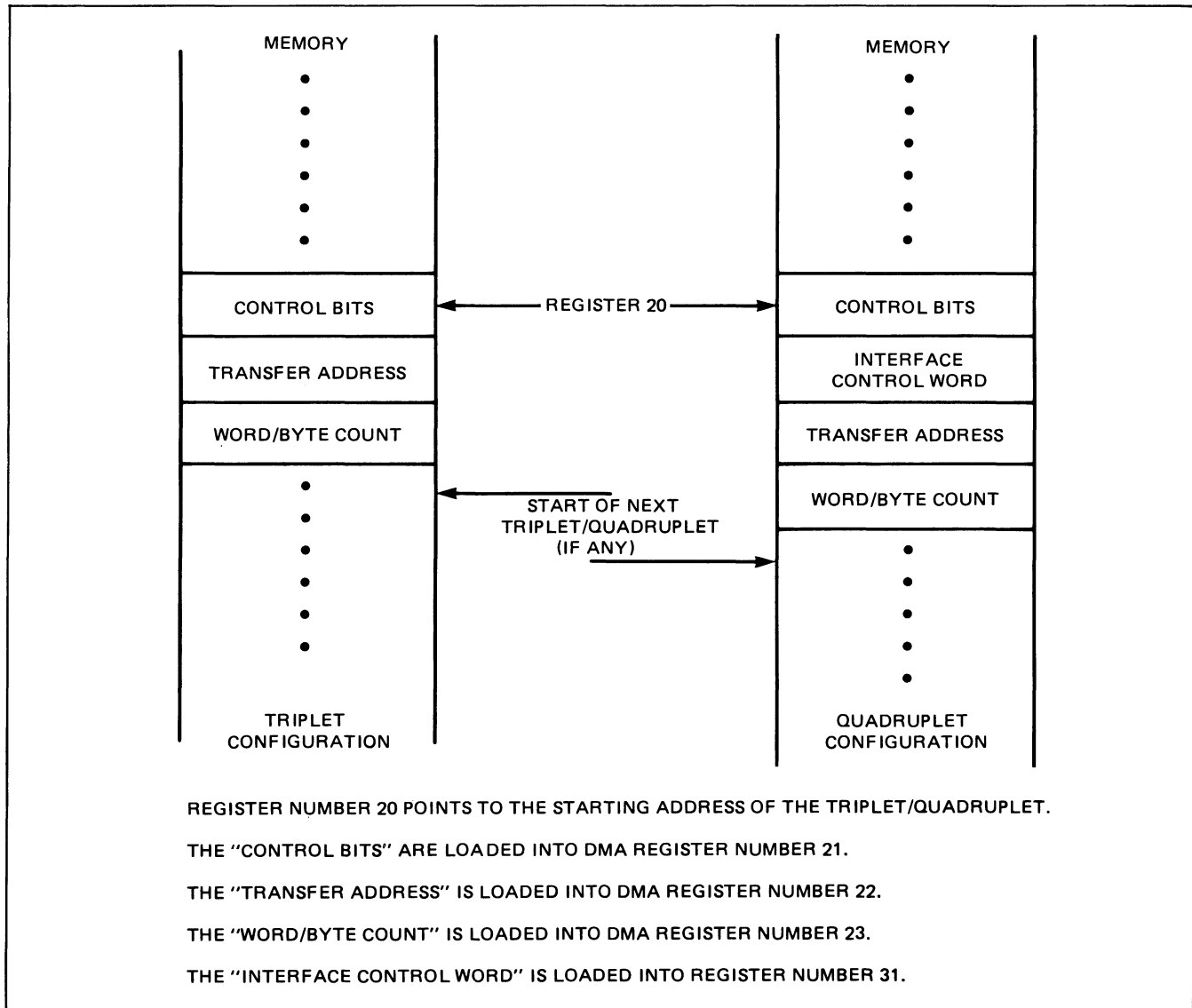


Figure 3-3. DMA Self-Configuration Feature

3-18. DMA SELF-CONFIGURATION FEATURE

Also available in the I/O chip is circuitry that enables the DMA registers (discussed in the preceding paragraphs) to be loaded directly from sequential memory locations. Upon completion of each successive DMA operation, the contents of register 20 are used as a pointer to the location in memory containing the next set of values to be loaded into registers 21, 22, and 23. As each register is loaded, the contents of register 20 are incremented, leaving register 20 pointing to the values to be used for the next transfer.

3-19. DMA SELF-CONFIGURATION INITIALIZATION. The DMA self-configuration feature is initialized by setting the value of register 20 to the memory address of the first word of a list of DMA triplets or quadruplets. A triplet is of the form control bits, transfer address, word/byte count. The triplet words are the words to

be used in registers 21, 22, and 23, respectively. A quadruplet is of the form control bits, interface control, transfer address, word/byte count. The quadruplet words are to be loaded into registers 21, 31, 22, and 23, respectively. Bit 8 of the control word determines whether a triplet or quadruplet is used. See figure 3-3 for the formats of triplets and quadruplets.

Once the DMA self-configuration feature is initialized by setting the value of register 20 equal to the memory address of the first word of a list of DMA triplets or quadruplets, an STC to register 20 starts the feature. This STC to register 20 has the effect of simultaneously setting the control on registers 20 and 21 (to achieve an initial state for full execution).

3-20. DMA SELF-CONFIGURATION OPERATION. After receiving the STC on register 20, the self-configuration control logic fetches the word addressed by the contents of register 20 and loads this word into regis-

ter 21. Assume bit 7 of this word is set, signifying a quadruplet. The contents of register 20 are incremented during the memory access. The new value of register 20 is used as the address of the next memory read. This next word is loaded into the control register on the PIC by means of a virtual OTA 31 generated by the I/O chip. Register 20 then is incremented for the next read and this new data is loaded into register 22. Register 20 is used to address the fourth word of the current quadruplet. This fourth word is loaded into register 23. The value of register 20 is again incremented, pointing to the beginning of the next triplet/quadruplet. The DMA operation just loaded is then started as soon as the interface is ready (see paragraph 3-15). When the DMA operation terminates (see paragraph 3-18), if bit 11 of register 21 is clear, an interrupt request is generated. If the DMA operation terminated due to either an end-of-transfer indication from the interface or a word/byte count transition from -1 to 0, and bit 12 of register 21 is set, the DMA self-configuration logic writes the word-count residue into the location formerly occupied by the current DMA operation's word/byte count. Operation of the self-configuration feature is continued, as noted above, for the next triplet/quadruplet.

3-21. DMA SELF-CONFIGURATION TERMINATION. The operation of the DMA self-configuration feature continues as described in the preceding paragraphs until one of the following events occurs:

- a. A CLC to register number 20 is executed. This serves to inhibit the self-configuration logic from advancing its pointer to the next triplet/quadruplet, while still allowing the current DMA to continue. An STC to register number 20 allows the self-configuration feature to continue.
- b. A CLC to register 21 is executed. This stops the current DMA operation at its present state of operation.
- c. A CLC to register number 22 is executed. This aborts the current DMA operation and causes the self-configuration logic to advance to the next triplet/quadruplet. No interrupt is generated by the aborted transfer.
- d. A CLC to register number 23 is executed. This stops the operation of the self-configuration logic and aborts the transfer in progress.
- e. The first word of a triplet is read with the CONT bit clear, indicating that there are no further DMA triplets. This sets the flag on register number 20, which generates an interrupt request if the control flip-flop of register number 20 is set.

3-22. FORMAT SUMMARY

The following paragraphs contain a reference guide to all control and data word formats for the PIC.

3-23. OUTPUT CONTROL WORD, REGISTER 31

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TSTU	SPARE	DFS	DCL	PLV	LBV EN	IRQ EN	TSTL	SRM	DRM	SNS	CNT3	CNT2	CNT1	CNT0	

3-24. INPUT STATUS WORD, REGISTER 32

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TSTU	SLV	DMA ON-	PACK	CN T3	CN T2	CN T1	CN T0	TSTL	DFF	FLAG	DCSS	ST3	ST2	ST1	ST0

3-25. DMA SELF-CONFIGURATION, REGISTER 20

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
POINTER TO DMA TRIPLET/QUADRUPLET															

3-26. DMA CONTROL WORD 1, REGISTER 21

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CONT	DVC MD	BYTE	RES	CINT	REM	FOUR	AUTO	IN	SPARE	RESERVED FOR DMS					

3-27. DMA ADDRESS, REGISTER 22

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DMA ADDRESS															

3-28. DMA WORD/BYTE COUNT, REGISTER 23

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DMA WORD/BYTE COUNT															

3-29. DMA BYTE MODE DATA, REGISTER 30

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
1ST BYTE OF DATA TRANSFERRED								2ND BYTE OF DATA TRANSFERRED							

3-30. SAMPLE PROGRAMMED I/O ROUTINE

The following is an example of a programmed I/O driver. Assume that the global register has already been loaded and enabled.

```

I.O      NOP                      *OUTPUT CONTROL WORD
          OTA 31
          OTB 30                  *OUTPUT DATA WORD
          STC 30,C                *TRANSFER DATA IN OR OUT
          SFS 30                  *WAIT FOR TRANSFER COMPLETE
          JMP*-1
          LIA 30                  *GET DATA INPUT
          JMP I.O,I              *RETURN
          JSB ERROR

RCV      LDA 31                  *CONTROL WORD FOR RECEIVE
                                     MODE IS LOADED INTO A
          JSB I.O
          .
          .
          .
          .                       PROCESS DATA
          .
          .
          .

XMIT     LDA 31                  *CONTROL WORD FOR TRANSMIT
                                     MODE IS LOADED INTO A
          LDB                      *DATA BYTE IS LOADED INTO B
          JSB I.O
          .
          .
          .
          .

```

3-31. PARALLEL INTERFACE CARD INITIALIZATION

The PIC responds to three different types of resets. There are two system resets, one of which occurs on power up and the other on execution of a CLC 0. When either of these events occurs, a reset signal is generated throughout the entire computer system, forcing every card into a known state. In many cases it may be desirable to reset the PIC card without performing a system reset. The third type of reset, which is an OTA 32 with the global register pointing to the PIC, accomplishes this. (The value of the A register is inconsequential to the reset operation.)

All three resets have exactly the same effect. Namely, each reset clears the DMAON flip-flop, the Slave flip-flop, the SRQ flip-flop, and registers 30 (output only) and 31. When these two registers are clear, all data and control lines being driven by the PIC are high. This results in a power savings of several watts over normal operation of the card. It is good practice, therefore, to execute an OTA 32 whenever an exit from the driver is to be performed, or whenever the PIC is to remain idle over a period of time.

3-32. VIRTUAL CONTROL PANEL

NOTE

The Virtual Control Panel program (located in the processor card ROMs) does not provide for VCP operation with the parallel interface. The VCP program must be modified if the parallel interface is to be used as a VCP interface.

The Virtual Control Panel is an interactive program that replaces a conventional hardware front panel. Because the A/L-Series does not have a front panel, provision has been made so that an I/O interface card may be selected as the interface to a Virtual Control Panel. See Section II, paragraph 2-10 for instructions on selecting the PIC to be the Virtual Control Panel interface.

A device being used as the Virtual Control Panel (VCP) provides control and access to the CPU in a manner similar to a hardware console. It enables the operator to access the various registers (A, B, P, etc.), examine or change memory, or control execution of a program. The Virtual Control Panel program is located in a Read-Only Memory (ROM) located on the central processor card.

Only one card in the A/L-Series system can be selected as the VCP interface at any given time. The VCP mode can be entered in any one of three ways:

- a. After power up, the boot loading program is directed to the VCP ROM program in lieu of a boot routine.
- b. The VCP interface receives a signal from the VCP device, signifying that the VCP routine is to be entered. In the case of the PIC, this indication is the assertion of the Slave Request line.
- c. Certain software instructions can cause the VCP routine to be entered as follows:
 1. An STC 3 or HALT instruction causes the I/O interface card to simulate a Slave Request. The STC instruction does not cause a Memory Protect violation, thus maintaining the system when the VCP program is entered.
 2. A CLC 3 instruction causes a simulated Slave Request after four instructions are executed. The CLC 3 instruction is used by the VCP program to allow the operator to single step through instructions.

When the PIC is used as the Virtual Control Panel interface, its select code must be set to 20 (octal).

3-33. SUMMARY OF I/O INSTRUCTION USAGE

The following paragraphs contain a summary of the usage by the PIC of eight I/O instructions, as follows: OTA, OTB, LIA, LIB, STC, CLC, STF, and CLF. Please see the A/L-Series I/O interfacing guide, part number 02103-90005, for a more comprehensive description.

3-34. OTA/OTB

Without the global register enabled, an OTA/OTB to the select code of the PIC will transfer data to the peripheral device. In order to control information to the PIC, the global register must be set up and enabled. An OTA/OTB to select code 2 loads the global register. Under global register control, the register addresses are defined as follows:

- OTA/OTB 2 Controls diagnostic mode of PIC (See Section V).
- OTA/OTB 20 Transfers self-configuring DMA starting address to PIC.
- OTA/OTB 21 Transfers DMA control word (see paragraph 3-8) to PIC.
- OTA/OTB 22 Transfers DMA starting address to PIC.
- OTA/OTB 23 Transfers DMA word or byte count to PIC.
- OTA/OTB 30 Transmits data to peripheral device.
- OTA/OTB 31 Transfers control word (see paragraph 3-5) to PIC.
- OTA/OTB 32 Performs a card reset.

3-35. LIA/LIB

Without the global register enabled, an LIA/LIB to the select code of the PIC will input data from the device. In order to fetch status information, or to read back any of the control registers, the global register must be set up and enabled. Under global register control, the register addresses are defined as follows:

- LIA/LIB 20 Reads next address to be used by DMA self-configuration feature. It is advisable to perform a CLC 20 before reading this register in order to insure its accuracy.
- LIA/LIB 21 Reads the DMA control word (see paragraph 3-8) from PIC.
- LIA/LIB 22 Reads the next DMA address. It is advisable to perform a CLC 21 before reading this register in order to insure its accuracy.
- LIA/LIB 23 Reads the remaining word or byte count. Again, it is advisable to perform a CLC 21 first.

LIA/LIB 30 Inputs data from the peripheral device.

LIA/LIB 32 Reads the PIC input status word (see paragraph 3-6).

3-36. STC

Without the global register enabled, an STC to the select code of the PIC serves to set the PICs Control flip-flop (located in the I/O chip), thereby enabling interrupts, and to generate a Device Command (DVCMD) signal. Under global register control, an STC has various meanings defined as follows:

- STC 20 Enables the DMA self-configuration feature. An STC with the Clear Flag bit set starts the transfer (see paragraph 3-19).
- STC 21 Enables a normal DMA transfer. With the Clear Flag bit set, STC 21 also starts the transfer (see paragraph 3-15).
- STC 30-77 Sets the PIC Control flip-flop, enabling non-DMA interrupts. Also generates a Device Command (DVCMD) signal.

3-37. CLC

Without the global register enabled, a CLC to the select code of the PIC has the same effect as a CLC 30-77 as defined below. A CLC 3 (select code 3) will invoke the Virtual Control-Panel, which only affects the PIC if it is set to operate in this mode (see paragraph 3-33). A CLC 0 generates a system reset signal (see paragraph 3-32). Under global register control, a CLC has various meanings defined as follows:

- CLC 20 Suspends the operation of the DMA self-configuration logic. Does not suspend current DMA operation.
- CLC 21 Suspends the operation of the current DMA transfer.
- CLC 22 Aborts the current DMA transfer. If self-configuration feature is enabled, proceed to next transfer in the self-configuration list.
- CLC 23 Aborts the DMA self-configuration feature and any transfer in progress.
- CLC 30-77 Resets the PIC Control flip-flop, disabling interrupts.

3-38. STF

Without the global register enabled, a STF to the select code of the PIC sets the FLAG flip-flop (located in the I/O

chip). An STF 2 disables global register operation. Under global register control, an STF has various meanings defined as follows:

- | | |
|--------|---|
| STF 20 | Sets the DMA self-configuration Flag flip-flop. |
| STF 21 | Sets the DMA Flag flip-flop. |

STF 30-77 Sets the PIC Flag flip-flop.

3-39. CLF

Without the global register enabled, a CLF to the select code of the PIC clears the Flag flip-flop. A CLF 2, or any instruction to select code 2 with the Clear Flag bit set, enables global register operation.

THEORY OF OPERATION

SECTION

IV

4-1. INTRODUCTION

The parallel interface card is a multi-purpose interface card designed to transfer data between the processor or memory and a peripheral I/O device. A single parallel interface card can be used to transfer data between from one to sixteen different devices by using the four control lines as address bits.

The PIC is composed of two sections: an I/O master section and a peripheral device interface section. The I/O master performs all of the I/O processing functions, including I/O instruction recognition and execution, direct memory accessing (DMA), and Virtual Control Panel (slave) mode processing. The I/O master consists of a 64-pin SOS (silicon-on-sapphire) chip, some Schottky memory request logic, and data bus, address bus, and I/O chip buffers. The printed circuit layout of the I/O master is standard for all A/L-Series I/O cards and occupies approximately one third of the card near the backplane connectors P1 and P2.

Figure 4-1 shows the PIC in a typical HP 1000 A/L-Series system. As shown, the PIC can be installed in any I/O slot (an I/O slot is any slot below the processor card in the backplane), and then connected by a cable to the peripheral device.

A six-bit select code for the PIC is set by a dual in-line package switch (U1) located on the PIC. The switch package consists of eight individual switches and is considered part of the I/O master. Six of the switches are used for the select code. The select code is used only as a means of addressing the card (and the peripheral device to which it is connected) and bears no relation to interrupt and DMA priority of the PIC. Interrupt and DMA priority are determined solely by the physical location of the PIC in the card cage. The card nearest the processor has highest priority, the card farthest away from the processor has lowest priority.

4-2. BASIC PIC OPERATION

The simplified block diagram shown in Section I, figure 1-2 illustrates the basic operation of the PIC in the computer system.

The I/O master, consisting of the I/O chip and other backplane interface logic, performs all interaction with the backplane. This includes decoding and executing I/O instructions and direct memory access (DMA) operations.

For a complete description of the I/O master, see the HP 1000 L-Series Computer Interfacing Guide, part no. 02103-90005.

A set of transceivers (U55, U65) buffer data from the backplane data bus to an internal bus on the PIC; or, in the case of data from the peripheral device, from the PIC internal bus to the backplane data bus.

Two data registers are provided on the card. The data output register (U43, U93) buffers data from the computer to the device, and the data input register (U53, U83) buffers data from the device to the computer. There are two principal control signals, Device Command and Device Flag. The Device Command signal effectively turns on the peripheral device and the Device Flag signal is sent back by the device to indicate either the completion of an output operation or the initiation of an input operation.

A 16-bit control register (U44, U84) on the card can be programmatically loaded. Four bits from this register are used to send control information to the peripheral device. These four bits may be used for such purposes as flexible disc control, or, as noted above, as address lines to select one of up to 16 devices connected to the PIC.

Additionally, there are four bits of status information from the device. These four bits are part of the 16-bit input to the status register (U54, U64) and are available to the programmer to determine device status.

4-3. DATA TRANSFER

The PIC transfers either 8 or 16 bits at a time in parallel. Usually, the PIC is connected to a unidirectional device such as a line printer or tape reader, and uses the Device Command/Device Flag handshake protocol to control the data transfer. With this method, the PIC is capable of up to a 1 MHz DMA transfer rate.

The PIC also can be used in environments where there is no Device Flag/Device Command handshake needed. An example of this type of application is when the 16 data input lines are connected to 16 different digital measurement devices or sensors. Instead of being clocked, the 16 bits of information are dynamically available to the user.

Finally, the PIC can be connected to another PIC and used for computer-to-computer communications. In this configuration, for example, the PIC could be used as the Virtual Control-Panel interface (see paragraph 4-9).

4-4. DATA TRANSFER SIGNALS. All data transfers involve the signals Service Request (SRQ), Service Request Acknowledge (SACK), Clock Data (CKDAT), Bus Control State 1 (BCS1) (for output data transfers), and Bus Control State 5 (BCS5) (for input data transfers).

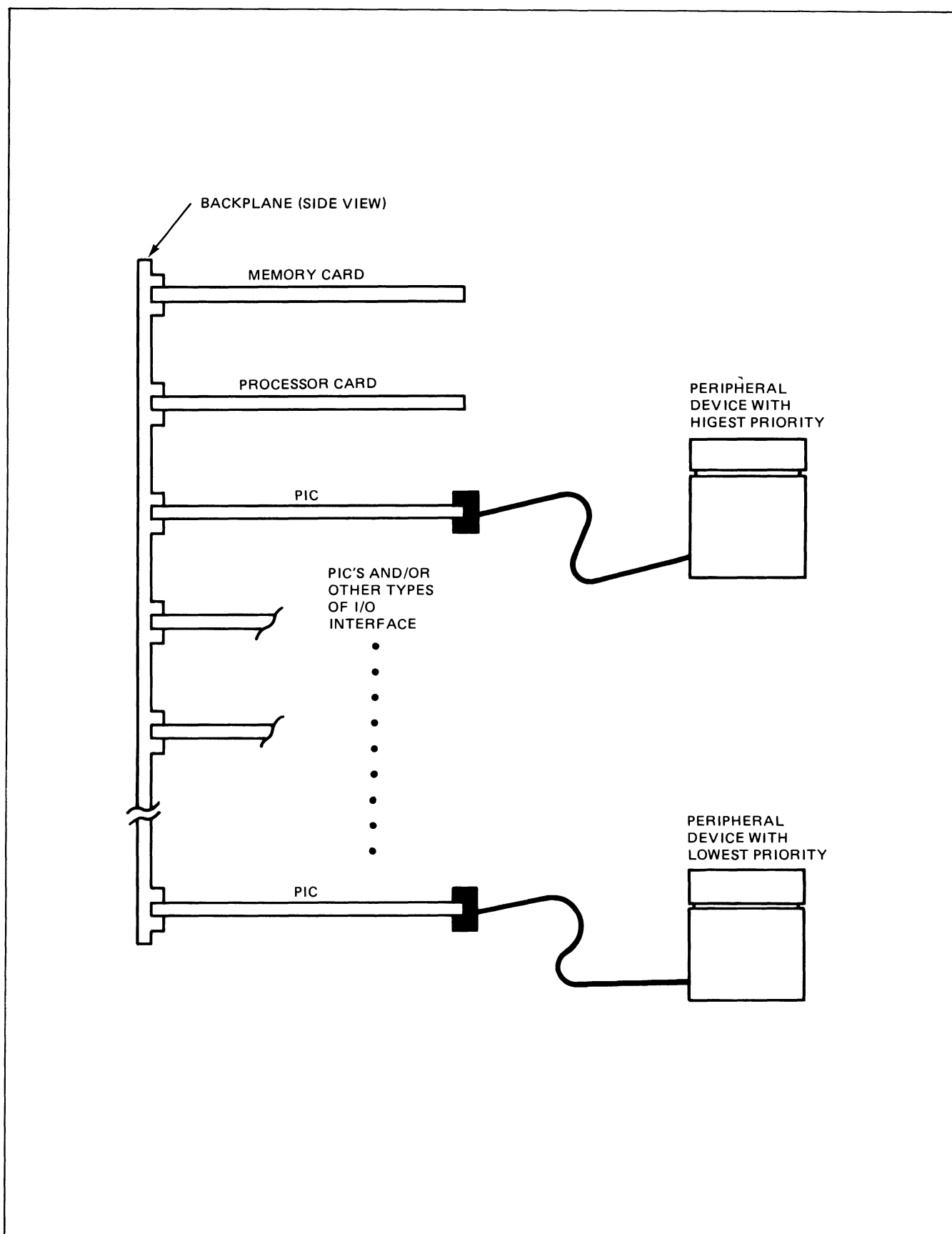


Figure 4-1. Parallel Interface Card in Typical System Environment

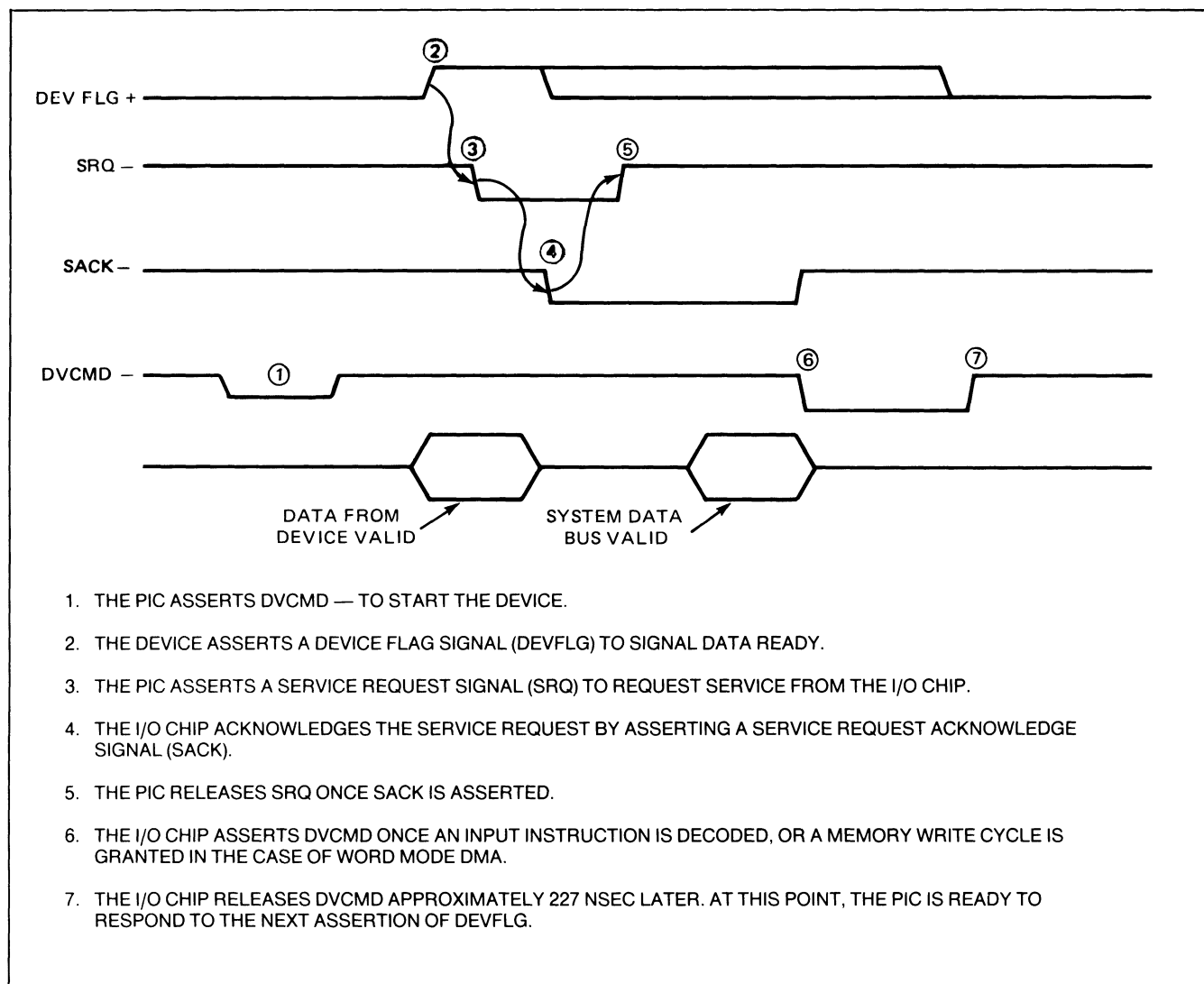


Figure 4-2. Input Transfer Timing

Additional signals are required depending on whether the transfer is an input, output, and/or DMA operation. These signals are described in the following paragraphs.

4-5. INPUT OPERATION. An input operation is defined as the transfer of data from a peripheral device to the computer. The protocol for this type of transfer is illustrated in figure 4-2. A Device Command (DVCMD) signal must be issued in order to start the device. The data transfer then proceeds as shown in figure 4-2.

4-6. OUTPUT OPERATION. An output operation is defined as a data transfer from the computer to a peripheral device. The protocol for an output transfer is illustrated in figure 4-3.

4-7. DMA OPERATION. Direct memory access operation bypasses the central processor; the PIC controls

the peripheral device to which it is connected and controls all data transfers between this device and memory.

DMA transfers involve all the data transfer handshake signals, and in addition, DMAEN, LOBYT, and LSBYT. Figures 4-4 through 4-8 show the various types of DMA transfers and how the appropriate signals are used. For most applications, and for most slow- and medium-speed peripherals, the DMA speed is not time-critical, because the peripheral's highest speed cannot approach the DMA rate. For these slow- to medium-speed applications, there are no timing constraints on the length of time that SRQ is asserted and on the use of DVCMD.

For high speed applications, however, where full DMA speed is desired, SRQ must be released within ($t - 80$ nsec) after the leading edge of SACK, where t is the duration of one long half cycle of SCLK (System Clock). Word mode DMA must be used in order to obtain back-to-back memory cycles. An absolute DMA rate cannot be guaranteed,

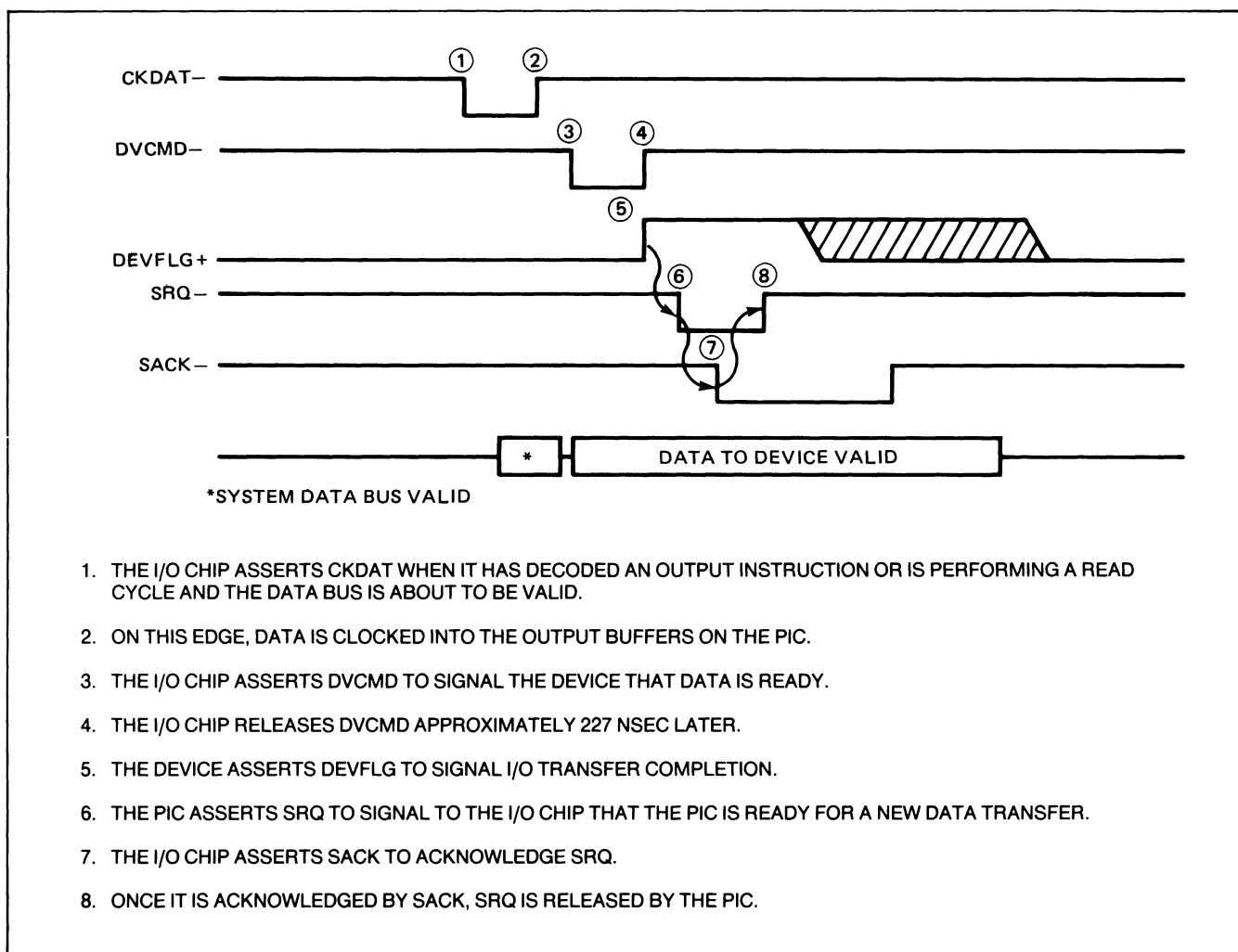


Figure 4-3. Output Transfer Timing

however, unless the PIC has the highest DMA transfer priority (that is, is the card nearest the processor in the card cage).

4-8. INTERRUPT HANDLING

Interrupt handling involves the signals Interrupt Request (IRQ) and Control Flip-Flop (CFF). The IRQ signal is issued to the I/O chip when the device detects an interrupting condition, and this feature has been enabled by bit 8 or Register 31. This sets the Flag flip-flop in the I/O chip, causing Flag 30 to get set. If CFF is asserted (Control flip-flop is set), an interrupt will be generated. Regardless of the state of CFF, Flag 30 will stay set until cleared programmatically.

4-9. VIRTUAL CONTROL PANEL OPERATION

The Virtual Control Panel (VCP), or slave-mode, operation involves the signals Slave Request (SLRQ) and Slave Acknowledge (SLAK).

The VCP is an interactive program that enables a peripheral device (or a remote computer) to control the central processor in a manner similar to conventional hardware front panel. That is, it allows the operator to access the various registers (A, B, P, etc.), examine or change memory, and control execution of a program. The VCP program is stored in read-only memory (ROM) on the central processor card.

NOTE

The Virtual Control Panel program (located in the processor card ROMs) does not provide for VCP operation with the parallel interface. The VCP program must be modified if the parallel interface is to be used as a VCP interface.

Note that the select code of the PIC must be set to 20 (octal) when it is to function as the Virtual Control Panel interface.

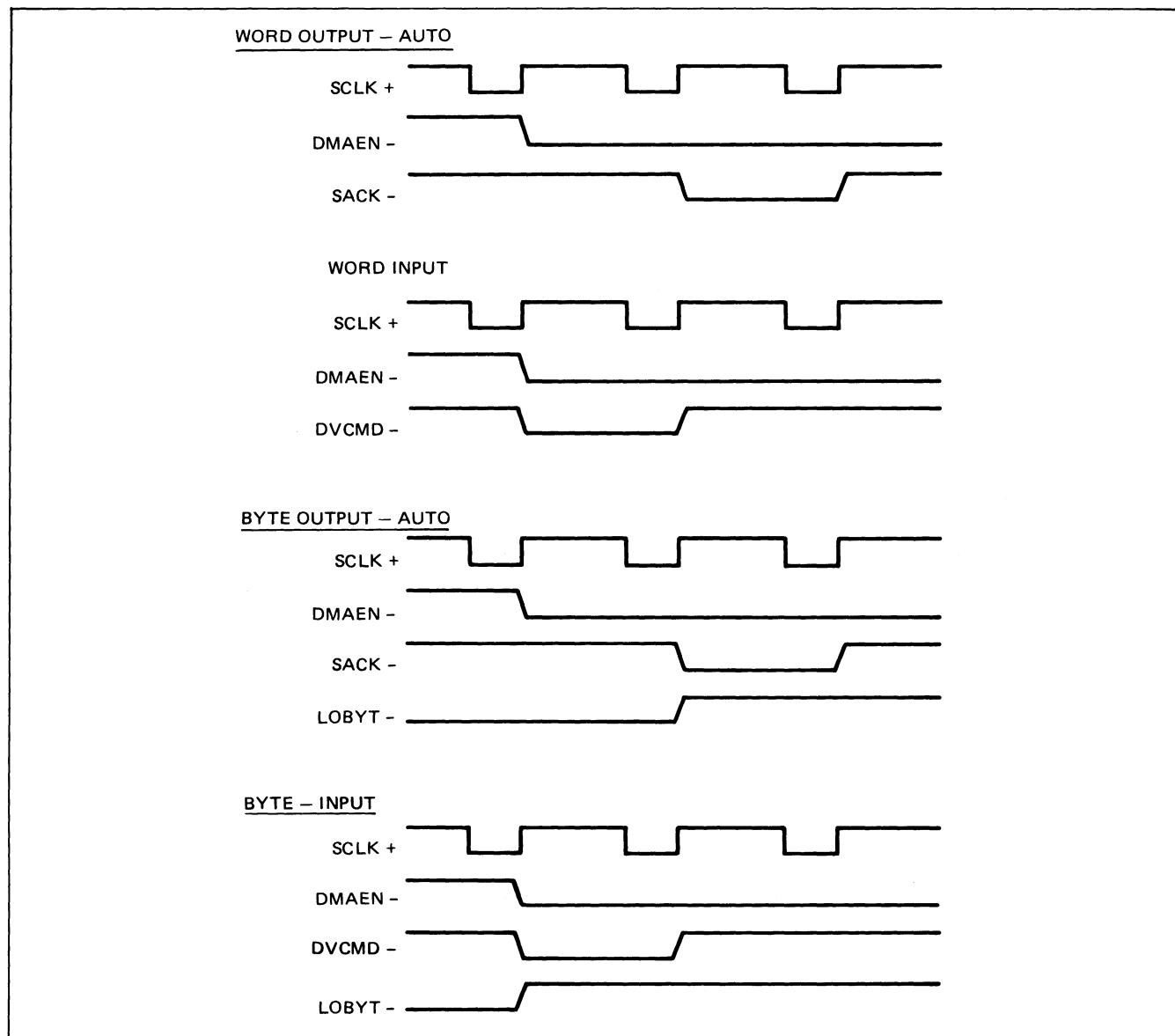


Figure 4-4. DMA Start-Up Sequence

Only one I/O card at a time can be enabled to respond to SLRQ. Whenever an I/O card wants to enter the VCP mode, it issues an SLRQ to its I/O chip. The I/O chip then forces the processor into the slave mode. The SLRQ flip-flop on the PIC can be cleared with an OTA32.

4-10. FUNCTIONAL THEORY OF OPERATION

The following paragraphs contain functional theory of operation for the PIC. A detailed functional block diagram is shown in Section VII, figure 7-2. Reference also should be made, as necessary, to the schematic logic diagram contained in figure 7-4.

4-11. PRINCIPAL DATA PATHS

The I/O chip bus is a 16-bit bi-directional bus over which all data is transferred between the backplane and the I/O chip. The I/O chip receives and drives the backplane data bus and drives the address bus. For example, each instruction fetched by the CPU is sent into the I/O chip via the chip bus; during DMA transfers, the transfer address is read out of the I/O chip via the chip bus.

Tri-state receivers and drivers provide bus-to-bus isolation and drive capability, as follows:

- U57, U58: Data from backplane data bus to chip bus.
- U47, U48: Data from chip bus to backplane data bus.

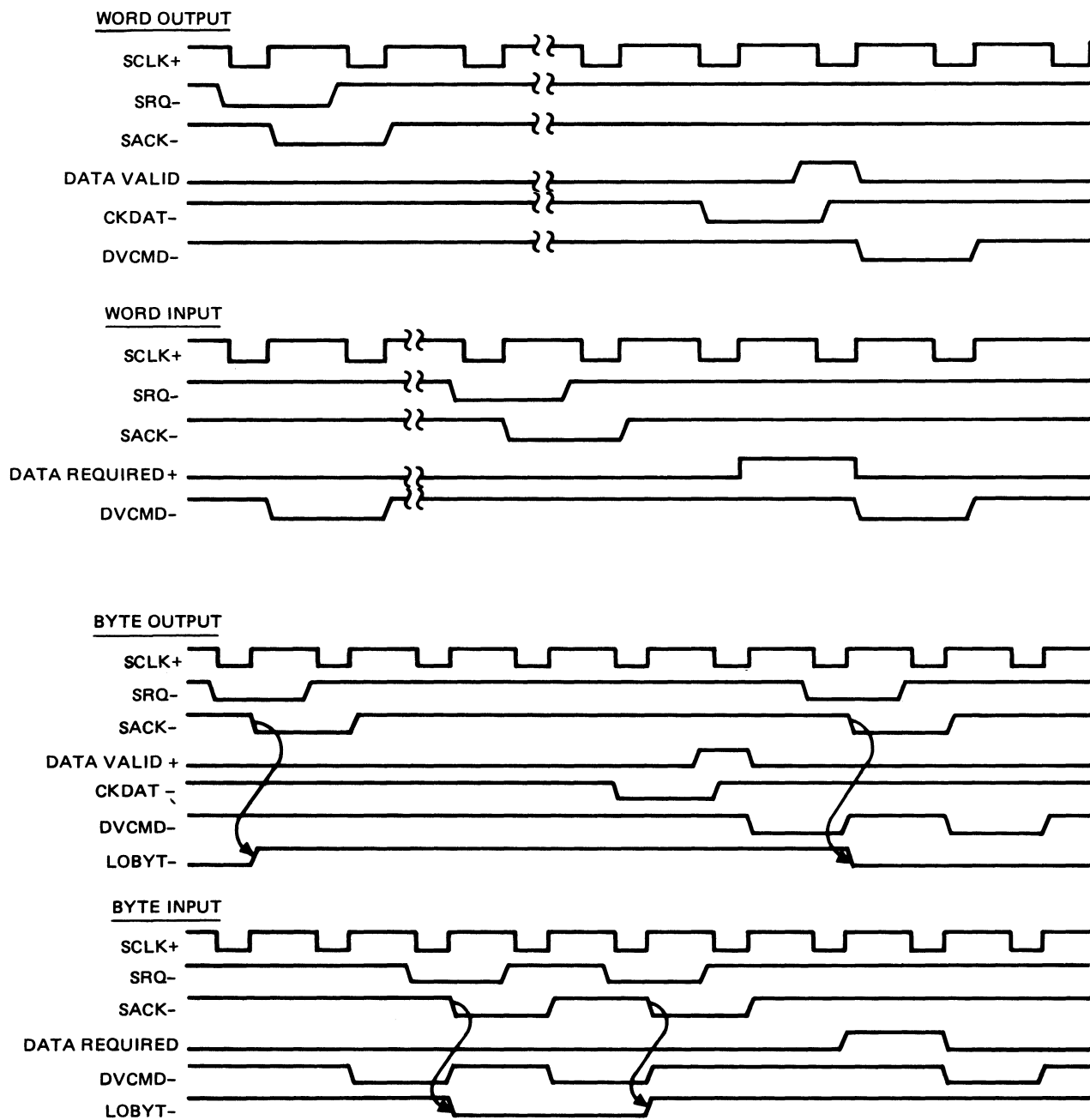
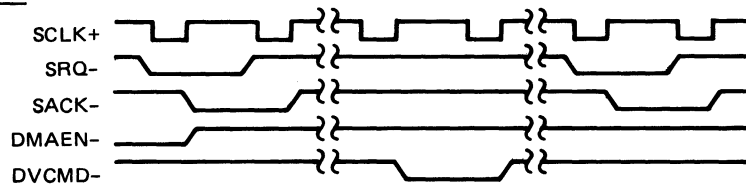
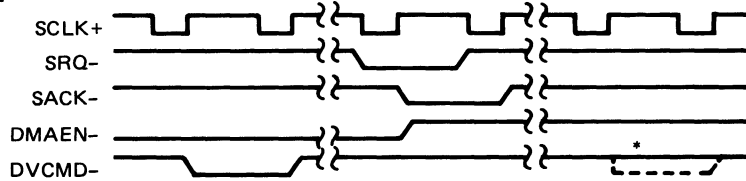


Figure 4-5. DMA In-Progress Sequence

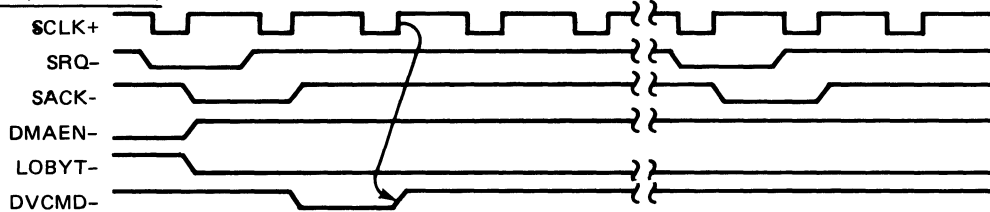
WORD OUTPUT



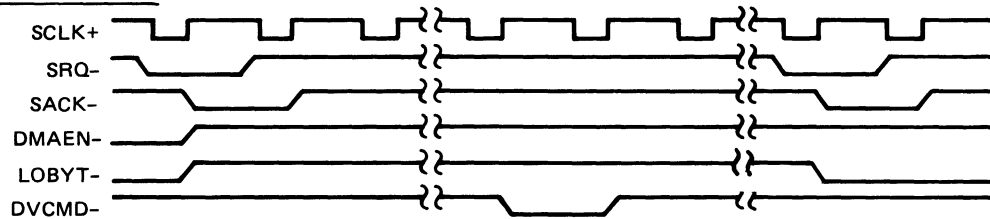
WORD INPUT



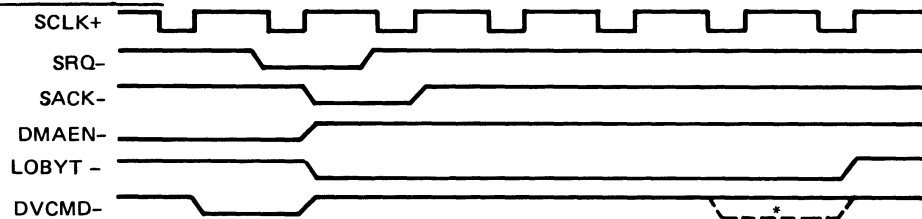
BYTE OUTPUT (EVEN BYTE)



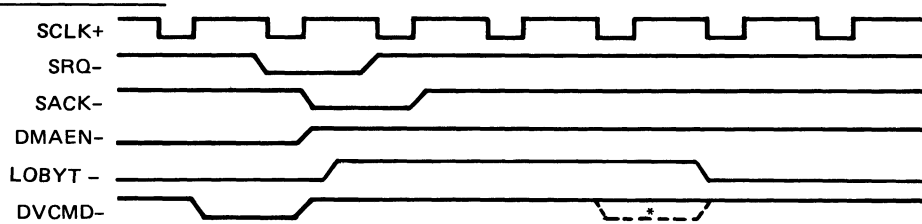
BYTE OUTPUT (ODD BYTE)



BYTE INPUT (EVEN BYTE)



BYTE INPUT (ODD BYTE)



*IF AUTO BIT SET IN REGISTER 31

Figure 4-6. DMA Termination Sequence

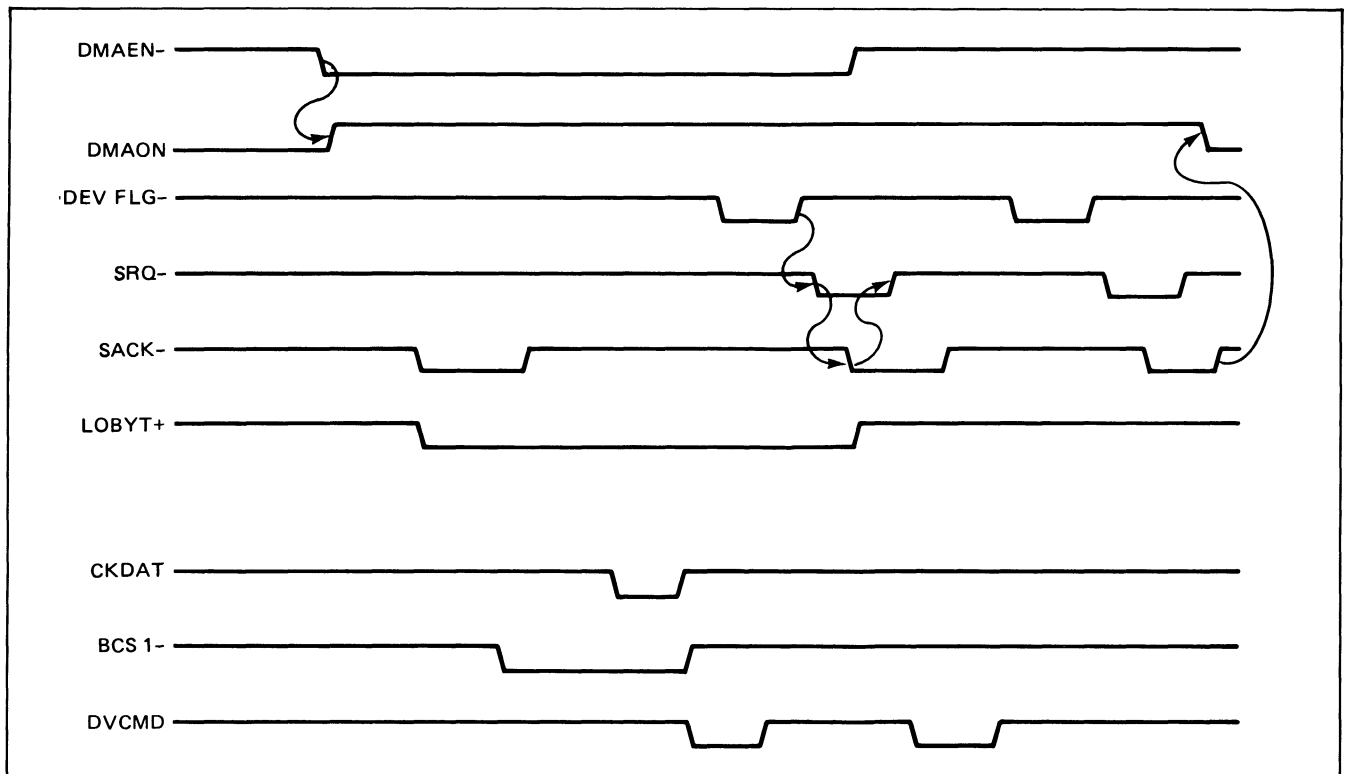


Figure 4-7. Two-Byte DMA Output Transfer Timing Diagram

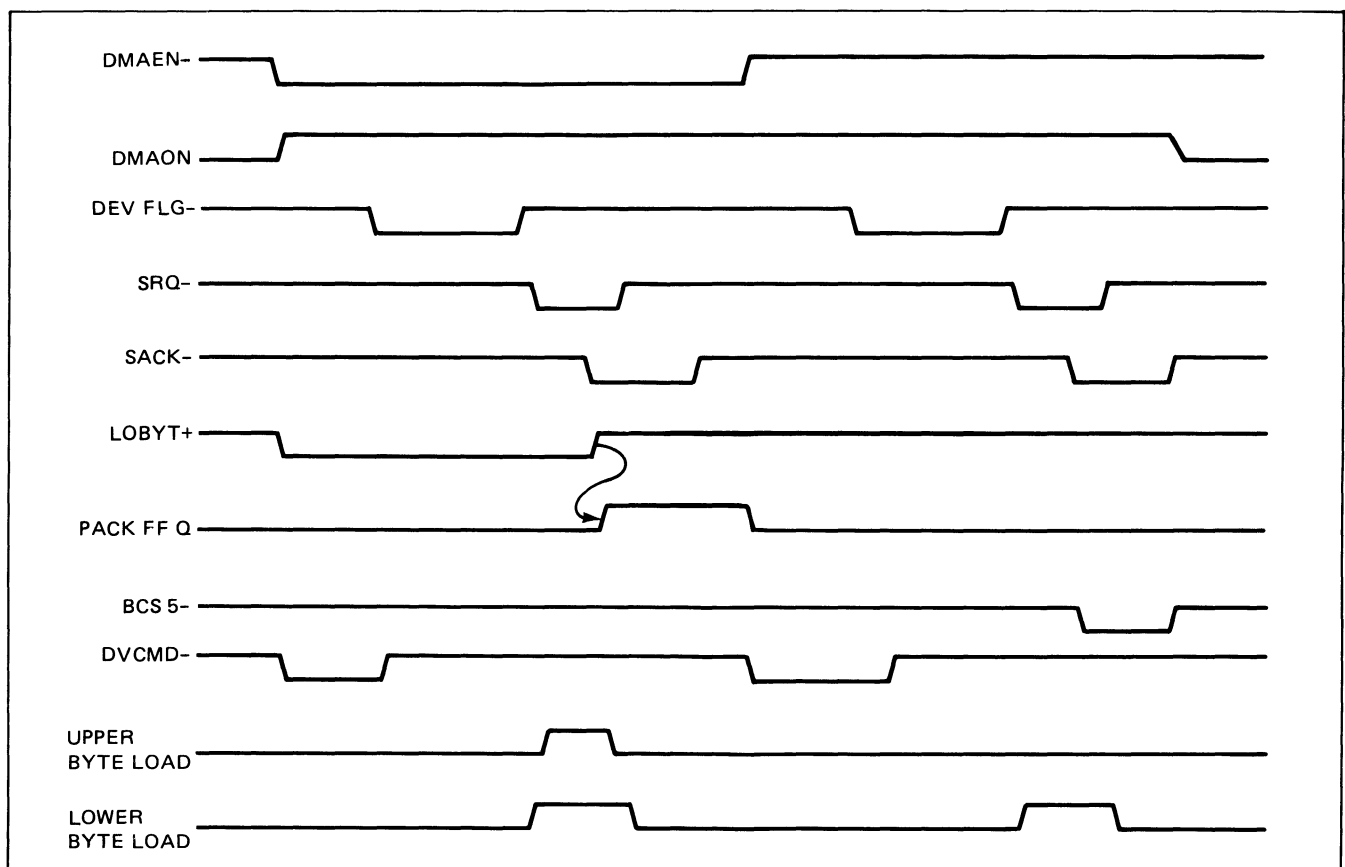


Figure 4-8. Two-Byte DMA Input Transfer Timing Diagram

- c. U37, U38: Address from chip bus to backplane address bus.
- d. U27, U28: Card ID code (used in diagnostic mode) to address bus via U37, U38.
- e. U18: Address bus extension from chip bus to backplane.

All data bus and internal bus management is controlled by the I/O chip (U67) and a state decoder (U46). While executing I/O instructions or executing DMA, the I/O chip controls the buses by asserting any one of several bus control state signals (BCS0-BCS7) which indicate when to latch or drive the buses. For example, BCS5 drives the data input register onto the data bus. BCS5 is asserted whenever an LIA instruction with the PIC's select code is executed and whenever the PIC is performing a write to memory during DMA input. When BCS5 is asserted, the data input register (U53, U83) is enabled onto the internal bus, and the bus transceivers (U55, U65) drive the internal bus onto the backplane data bus.

4-12. OUTPUT DATA PATH. The bus control signal BCS1 loads the data output register. Once loaded, the data must be sent to the peripheral device. If DMA is executing in byte-mode output, the data must be unpacked into 8-bit bytes. The two multiplexers, U13 and U23, perform this function. The upper byte is sent to the device first, so at that time, LOBYT- (Low Byte), a signal from the IOP chip, is high (is not asserted), thus multiplexing bits 15 - 8 into bits 7 - 0 of the output drivers. This sends the high byte to the peripheral device. After the next Device Flag signal, LOBYT- switches (is asserted), multiplexing bits 7 - 0 into bits 7 - 0 of the output drivers, thus sending the lower byte to the peripheral device. Figure 4-7 contains a timing diagram for a two-byte DMA output transfer.

Before the output driver stage (U11, U21, U31, U41, U51, U61, U71, and U81), 16 exclusive OR gates (U12, U22, U32, and U92) pass the data, with one input of each XOR gate driven by the control register. By this means, the data may be selectively inverted for devices which require ground true data.

4-13. INPUT DATA PATH. The 16 data input lines are connected directly to a set of 16 exclusive OR gates (U42, U52, U62, and U72), so that the data may be inverted when interfacing to a ground true device. The outputs of the exclusive OR gates are connected to two multiplexers (U63, U73). During byte packing, bits 0 - 7 of the data input then can be latched into the upper byte input buffer (U83). A timing diagram for a two-byte DMA input transfer is shown in figure 4-8.

4-14. DEVICE COMMAND/DEVICE FLAG INTERACTION

The DEVCOM flip-flop (U105) can be set only by a DVCMD signal from the IOP chip which is asserted upon

execution of an STC instruction and, in addition, on every DMA transfer. During non-DMA operation, the DEVCOM flip-flop may be cleared by a CLC instruction, and is held clear when the Control flip-flop (located in the I/O chip) is not set. In either case (DMA or non-DMA), the DEVCOM flip-flop is cleared by the DEVFLG signal from the peripheral device. The DEVCOM flip-flop can be clocked off by either edge of DEVFLG. The edge is selectable by bit 11 of control register 31 (if bit 11 = 1, DEVCOM flip-flop will clear on the opposite edge of DEVFLG than that which caused SRQ; if bit 11 = 0, DEVCOM flip-flop will clear on the same edge of DEVFLG which caused SRQ).

The DEVFLG signal from the peripheral device often contains significant noise, and therefore the PIC contains an RC noise filtering circuit on the Device Flag line with a time constant of approximately 250 nsec. This is large enough to filter out the noise introduced on the line by slower devices, while at the same time being small enough to permit 1 MHz DMA transfer rates.

4-15. MODE SELECTION

Bits 5 and 6 in control word 31 can be used to select transparent latch or clocked mode for the status register 32 (U54, U64) and data input register 30 (U53, U83). If bit 5 = 1, data register 30 is loaded on each DEVFLG signal from the peripheral device. If bit 5 = 0, data register 30 acts as a transparent latch; that is, all 16 bits are dynamically available. The transparent latch mode of operation is used when the PIC is connected to devices such as monitoring or measuring sensors.

If bit 6 = 1, status register 32 is loaded on each DEVFLG signal from the peripheral device. If bit 6 = 0, status register 32 acts as a transparent latch so that the status is dynamically available.

The two lines from control register 31, bits 5 and 6, are connected to the Mode multiplexer (U34). When the transparent latch mode is selected, the system clock is selected by the multiplexer, so that the control and status registers are clocked approximately every 225 nsec, or at whatever speed SCLK is running. Because these registers are clocked more frequently than data or status can be input, they appear as transparent latches to the user. Note that byte packing cannot be used while the data register is in transparent latch mode, and that DMA can only be used if there is a method of generating SRQ, that is, if DEVFLG is used.

When clocked mode is selected, the data and status registers are clocked by an edge of DEVFLG selectable by bit 12 of control register 31. Note that this will be the same edge that causes the assertion of SRQ.

The only critical timing involved in clocking the data input registers is the clocking of the upper byte while byte packing is in effect. The lower byte can be clocked every time DEVFLG is asserted, and overwritten when the low byte is received. The upper byte, however, must be clocked

at all times except when byte packing is enabled and LOBYT⁻ is low. In order to determine when this situation exists, the PACK flip-flop (U74) is used to remember when a DMA transfer is in progress and packing is used. The Q output of this flip-flop is NAnDED with LOBYT⁺ (U94) so that the upper byte clock is disabled when the Pack flip-flop Q output and LOBYT⁺ are both high.

4-16. SLAVE MODE OPERATION

The Slave Request signal from the peripheral device goes to the SLAVE flip-flop. The signal has a resistor pull-up (330 ohms), and the signal must be set low by any device wishing to enter slave mode. The pull-up resistor's value is low so that the Slave Request signal won't be falsely asserted in a noisy environment.

When Slave Request is asserted, the Slave flip-flop is set. This generates an SLRQ (Slave Request) signal to the I/O chip. If the Virtual Control Panel switch was enabled on power up (selecting the PIC as VCP interface), the I/O master then forces the processor into slave mode. If the VCP was not enabled on power up, the Slave Request signal is ignored. The Slave flip-flop may be cleared by execution of an OTA 32.

4-17. PIC-TO-PERIPHERAL DEVICE SIGNAL DEFINITIONS

Table 4-1 contains PIC-to-peripheral device signal definitions. Information for each signal includes: the signal mnemonic, its full name, where it originates, where it goes to, and what its function is.

Table 4-1. PIC/Peripheral Device Signal Definitions

NOTE

When delivered, the PIC is configured for +5V device interface. All device lines are terminated so that the +5V is best for high-speed applications such as computer-to-computer communications.

In order to configure the PIC for +12V device interface (devices such as paper tape readers and punches), remove the six resistor packages (R6, R7, R8, R9, R10, and R11) from the three 20-pin

Table 4-1. PIC/Peripheral Device Signal Definitions (Continued)

sockets along the front plane of the card. See figure 7-3 for the physical locations and figure 7-4 for the circuit locations of these resistors.

MNEMONIC: CNT0 - CNT3
FULL NAME: Control 0 (least significant bit) through Control 3 (most significant bit)
DRIVEN BY: Control register (U44)
RECEIVED BY: Peripheral device
FUNCTION: Device control

MNEMONIC: DVCMD
FULL NAME: Device Command
DRIVEN BY: DVCMD flip-flop
RECEIVED BY: Peripheral device
FUNCTION: Signals a data transfer request

MNEMONIC: DEVFLG
FULL NAME: Device Flag (Service Request)
DRIVEN BY: Peripheral device
RECEIVED BY: SRQ flip-flop
FUNCTION: Clocks DVCMD off and signals PIC that peripheral device is ready to transfer data.

MNEMONIC: IN0 - IN15
FULL NAME: Data from device 0 (least significant bit) through 15 (most significant bit)
DRIVEN BY: Peripheral device
RECEIVED BY: Data input buffer (U53, U83)
FUNCTION: Data from peripheral device

MNEMONIC: OUT0 - OUT15
FULL NAME: Data to device 0 (least significant bit) through 15 (most significant bit)
DRIVEN BY: Data output buffer (U43, U93)
RECEIVED BY: Peripheral device
FUNCTION: Data to device

MNEMONIC: SLRQ
FULL NAME: Slave Request
DRIVEN BY: Peripheral device
RECEIVED BY: Slave flip-flop
FUNCTION: Requests slave-mode (Virtual Control Panel) operation

5-1. INTRODUCTION

This section provides maintenance information for the HP 12006A Parallel Interface. Included are preventive maintenance instructions and troubleshooting information.

5-2. PREVENTIVE MAINTENANCE

Preventive maintenance for the parallel interface is performed at the same intervals as for the computer system as a whole.

Preventive maintenance consists of inspecting the PIC for burned or broken components, or the presence of foreign material. The cable and connector which connect the PIC to the device should also be checked for damaged insulation, bent or broken pins, etc. After any damage has been repaired, run the system self-test. (Refer to the appropriate A-Series or L-Series Installation and Service Manual.) If it is determined that the PIC is malfunctioning, perform the troubleshooting procedures listed in paragraph 5-3.

5-3. TROUBLESHOOTING

To troubleshoot the PIC, perform the following steps:

1. Run the computer self-test. Refer to the appropriate Installation and Service Manual for your A-Series or L-Series computer.
2. Run the kernel diagnostic. Refer to the Kernel Diagnostic Operating Manual, part number 24612-90003.
3. Run the PIC diagnostic. Refer to the Parallel Interface Diagnostic Operating Manual, part number 24612-90004.
4. If the PIC is defective, contact the nearest Hewlett-Packard Sales and Service Office for information on repair or replacement of the PIC. (Sales and Service Offices are listed at the back of this manual.)
5. If desired, however, further isolation to a defective component may be performed using an oscilloscope. Refer to Section VII, figure 7-1 for integrated circuit pin connections and characteristics, to figure 7-3 for PIC part locations, and to figure 7-4 for a schematic logic diagram. Refer to Section VI, table 6-3 for replaceable parts information.

Refer to Section II, table 2-1 for backplane connections to connector P1, table 2-2 for backplane connections to connector P2, table 2-3 for PIC-to-peripheral device interconnecting cable connections, and table 2-4 for computer-to-computer communications cable connections.

REPLACEABLE PARTS

SECTION

VI

6-1. INTRODUCTION

This section contains information for ordering replaceable parts for the HP 12006A Parallel Interface. Table 6-1 is a list of commonly-used prefixes for component parts, table 6-2 lists the meanings of the reference designations and abbreviations used in the table of replaceable parts, table 6-3 is the list of replaceable parts, and table 6-4 contains names and addresses of manufacturers of the parts.

6-2. REPLACEABLE PARTS

Table 6-3 contains a list of replaceable parts in reference designation order. The following information is listed for each part:

- Reference designation of the part. Refer to table 6-2 for an explanation of the abbreviations used in the "REFERENCE DESIGNATION" column.
- The Hewlett-Packard part number.
- Part number check digit (CD).
- Total quantity (QTY).
- Description of the part.
- A five-digit manufacturer's code number of a typical manufacturer of the part.
- The manufacturer's part number.

6-3. ORDERING INFORMATION

To order replacement parts or to obtain information on parts, address the order or inquiry to the local Hewlett-Packard Sales and Service Office (Sales and Service Offices are listed at the back of this manual).

To order a part listed in the replaceable parts table, quote the Hewlett-Packard part number (with the check digit), and indicate the quantity required. The check digit will insure accurate and timely processing of your order.

To order a part that is not listed in the replaceable parts table, specify the following information:

- Identification of the product containing the part (refer to Section I, paragraph 1-5).
- Description and function of the part.
- Quantity required.

Table 6-1. Commonly-Used Prefixes for Component Parts

PREFIX	COMPONENT/PART/MATERIAL
0121-	Capacitors, Variable (mechanical)
0122-	Capacitors, Voltage Variable (semiconductor)
0140-	Capacitors, Fixed
0150-	Capacitors, Fixed Non-Electrolytic
0160-	Capacitors, Fixed
0180-	Capacitors, Fixed Electrolytic
0330-	Insulating Materials
0340-	Insulators, Formed
0370-	Knobs, Control
0380-	Spacers and Standoffs
0410-	Crystals
0470-	Adhesives
0490-	Relays
0510-	Fasteners
0674- thru 0778-	Resistors, Fixed (non wire wound)
0811- thru 0831-	Resistors (wire wound)
1200-	Sockets for components
1205-	Heat Sinks
1250-	Connectors (RF and related parts)
1251-	Connectors (non RF and related parts)
1410-	Bearings and Bushings
1420-	Batteries
1810-	Resistor Network, 10 pin
1820-	Monolithic Digital Integrated Circuits
1826-	Monolithic Linear Integrated Circuits
1853-	Transistors, Silicon PNP
1854-	Transistors, Silicon NPN
1855-	Field-Effect-Transistors
1900- thru 1912-	Diodes
1920- thru 1952-	Vacuum Tubes
1990-	Semiconductor Photosensitive and Light-Emitting Diodes
3100- thru 3106-	Switches
8120-	Cables
9100-	Transformers, Coils, Chokes, Inductors, and Filters

Table 6-2. Reference Designations and Abbreviations

REFERENCE DESIGNATIONS		
A = assembly B = motor, synchro BT = battery C = capacitor CB = circuit breaker CR = diode DL = delay line DS = indicator E = Misc electrical parts F = fuse FL = filter J = receptacle connector	K = relay L = inductor M = meter P = plug connector Q = semiconductor device other than diode or integrated circuit R = resistor RT = thermistor S = switch T = transformer	TB = terminal board TP = test point U = integrated circuit, non-repairable assembly V = vacuum tube, photocell, etc. VR = voltage regulator W = jumper wire X = socket Y = crystal Z = tuned cavity, network
ABBREVIATIONS		
A = amperes ac = alternating current Ag = silver Al = aluminum ar = as required adj = adjust assy = assembly b = base bp = bandpass bpi = bits per inch blk = black blu = blue brn = brown brs = brass Btu = British thermal unit Be Cu = beryllium copper cpi = characters per inch coll = collector cw = clockwise ccw = counterclockwise cer = ceramic com = common crt = cathode-ray tube CTL = complementary-transistor logic cath = cathode Cd pl = cadmium plate comp = composition conn = connector compl = complete dc = direct current dr = drive DTL = diode-transistor logic depc = deposited carbon dpdt = double-pole, double-throw dpst = double-pole, single-throw em = emitter ECL = emitter-coupled logic ext = external encap = encapsulated elctlt = electrolytic F = farads FF = flip-flop flh = flat head flm = film fxd = fixed filh = fillister head G = giga (10^9) Ge = germanium gl = glass gnd = ground(ed)	gra = gray grn = green H = henries Hg = mercury hr = hour(s) Hz = hertz hdw = hardware hex = hexagon, hexagonal ID = inside diameter IF = intermediate frequency in. = inch, inches I/O = input/output int = internal incl = include(s) insul = insulation, insulated impgrg = impregnated incand = incandescent ips = inches per second k = kilo (10^3), kilohm lp = low pass m = milli (10^{-3}) M = mega (10^6), megohm My = Mylar mfr = manufacturer mom = momentary mtg = mounting misc = miscellaneous met. ox. = metal oxide mintr = miniature n = nano (10^{-9}) nc = normally closed or no connection Ne = neon no. = number n.o. = normally open np = nickel plated NPN = negative-positive-negative NPO = negative-positive zero (zero temperature coefficient) NSR = not separately replaceable NRFR = not recommended for field replacement OD = outside diameter OBD = order by description orn = orange ovh = oval head oxd = oxide p = pico (10^{-12}) PC = printed circuit	PCA = printed-circuit assembly PWB = printed-wiring board phh = phillips head pk = peak p-p = peak-to-peak pt = point prv = peak inverse voltage PNP = positive-negative-positive pwv = peak working voltage porc = porcelain posn = position(s) pozi = pozidrive rf = radio frequency rdh = round head rms = root-mean-square rww = reverse working voltage rect = rectifier r/min = revolutions per minute RTL = resistor-transistor logic s = second SB, TT = slow blow Se = selenium Si = silicon scr = silicon controlled rectifier sst = stainless steel stl = steel spcl = special spdt = single-pole, double-throw spst = single-pole, single-throw Ta = tantalum td = time delay Ti = titanium tgl = toggle thd = thread tol = tolerance TTL = transistor transistor logic U(μ) = micro (10^{-6}) V = volt(s) var = variable vio = violet Vdcw = direct current working volts W = watts ww = wirewound wht = white WIV = working inverse voltage yel = yellow

Table 6-3. Replaceable Parts

Reference Designation	HP Part Number	C D	Qty	Description	Mfr Code	Mfr Part Number
	12006-60003	6	1	ASSEMBLY, PC PARALLEL	28480	12006-60003
C1	0160-4808	4	1	CAPACITOR-FXD 470PF +-5% 100 VDC CER	28480	0160-4808
C2	0160-4842	6	8	CAPACITOR-FXD .22UF +80-20% 50 VDC CER	28480	0160-4842
C3	0160-4842	6		CAPACITOR-FXD .22UF +80-20% 50 VDC CER	28480	0160-4842
C4	0160-4842	6		CAPACITOR-FXD .22UF +80-20% 50 VDC CER	28480	0160-4842
C5	0160-4842	6		CAPACITOR-FXD .22UF +80-20% 50 VDC CER	28480	0160-4842
C6	0160-4842	6		CAPACITOR-FXD .22UF +80-20% 50 VDC CER	28480	0160-4842
C7	0160-4842	6		CAPACITOR-FXD .22UF +80-20% 50 VDC CER	28480	0160-4842
C8	0160-4842	6		CAPACITOR-FXD .22UF +80-20% 50 VDC CER	28480	0160-4842
C9	0160-4842	6		CAPACITOR-FXD .22UF +80-20% 50 VDC CER	28480	0160-4842
E1	0360-1682	0	3	TERMINAL-STUD SGL-TUR PRESS-MTG	28480	0360-1682
E2	0360-1682	0		TERMINAL-STUD SGL-TUR PRESS-MTG	28480	0360-1682
E3	0360-1682	0		TERMINAL-STUD SGL-TUR PRESS-MTG	28480	0360-1682
R1	0757-0280	3	1	RESISTOR 1K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1001-F
R2	1810-0280	8	1	NETWORK-RES 10-PIN-SIP .1-PIN-SPCG	01121	210A103
R3	1810-0277	3	3	NETWORK-RES 10-PIN-SIP .1-PIN-SPCG	01121	210A222
R4	1810-0277	3		NETWORK-RES 10-PIN-SIP .1-PIN-SPCG	01121	210A222
R5	1810-0277	3		NETWORK-RES 10-PIN-SIP .1-PIN-SPCG	01121	210A222
R6	1810-0298	2	3	NETWORK-RES 10-PIN-SIP .1-PIN-SPCG	01121	210A240
R7	1810-0298	2		NETWORK-RES 10-PIN-SIP .1-PIN-SPCG	01121	210A240
R8	1810-0298	2		NETWORK-RES 10-PIN-SIP .1-PIN-SPCG	01121	210A240
R9	1810-0407	1	3	NETWORK-RES 10-PIN-SIP .1-PIN-SPCG	73138	785-5-R(330/470)
R10	1810-0407	1		NETWORK-RES 10-PIN-SIP .1-PIN-SPCG	73138	785-5-R(330/470)
R11	1810-0407	1		NETWORK-RES 10-PIN-SIP .1-PIN-SPCG	73138	785-5-R(330/470)
R12	0757-0417	8	1	RESISTOR 562	28480	0757-0417
R13	1810-0275	1	1	NETWORK-RES 10-PIN-SIP .1-PIN-SPCG	01121	210A102
U1	3101-2243	6	1	SWITCH, DIP, 8-ROCKER	28480	3101-2243
U11	1820-0535	7	11	IC DRVR TTL AND DUAL 2-INP	01295	SN75451BP
U12	1820-1211	8	11	IC GATE TTL LS EXCL-OR QUAD 2-INP	01295	SN74LS86N
U13	1820-1470	1	4	IC MUXR/DATA-SEL TTL LS 2-TO-1-LINE QUAD	01295	SN74LS157N
U18	1820-1997	7	3	IC FF TTL LS D-TYPE POS-EDGE-TRIG PRL-IN	01295	SN74LS374PC
U21	1820-0535	7		IC DRVR TTL AND DUAL 2-INP	01295	SN75451BP
U22	1820-1211	8		IC GATE TTL LS EXCL-OR QUAD 2-INP	01295	SN74LS86N
U23	1820-1470	1		IC MUXR/DATA-SEL TTL LS 2-TO-1-LINE QUAD	01295	SN74LS157N
U27	1820-2024	3	4	IC DRVR TTL LS LINE DRVR OCTL	01295	SN74LS244N
U28	1820-2024	3		IC DRVR TTL LS LINE DRVR OCTL	01295	SN74LS244N
U31	1820-0535	7		IC DRVR TTL AND DUAL 2-INP	01295	SN75451BP
U32	1820-1211	8		IC GATE TTL LS EXCL-OR QUAD 2-INP	01295	SN74LS86N
U34	1820-1244	7	1	IC MUXR/DATA-SEL TTL LS 4-TO-1-LINE DUAL	01295	SN74LS153N
U35	1820-1208	3	1	IC GATE TTL LS OR QUAL 2-INP	01295	SN74LS32N
U36	1820-1367	5	1	IC GATE TTL S AND QUAD 2-INP	01295	SN74S08N
U37	1820-2102	8	4	IC LCH TTL LS D-TYPE OCTL	01295	SN74LS373N
U38	1820-2102	8		IC LCH TTL LS D-TYPE OCTL	01295	SN74LS373N
U41	1820-0535	7		IC DRVR TTL AND DUAL 2-INP	01295	SN75451BP
U42	1820-1211	8		IC GATE TTL LS EXCL-OR QUAD 2-INP	01295	SN74LS86N
U43	1820-1730	6	4	IC FF TTL LS D-TYPE POS-EDGE-TRIG COM	01295	SN74LS273N
U44	1820-1730	6		IC FF TTL LS D-TYPE POS-EDGE-TRIG COM	01295	SN74LS273N
U45	1820-1201	6	2	IC GATE TTL LS AND QUAD 2-INP	01295	SN74LS08N
U46	1820-1240	3	1	IC DCOR TTL S 3-TO-8-LINE 3-INP	01295	SN74S138N
U47	1820-2024	3		IC DRVR TTL LS LINE DRVR OCTL	01295	SN74LS244N
U48	1820-2024	3		IC DRVR TTL LS LINE DRVR OCTL	01295	SN74LS244N
U51	1820-0535	7		IC DRVR TTL AND DUAL 2-INP	01295	SN75451BP
U52	1820-1211	8		IC GATE TTL LS EXCL-OR QUAD 2-INP	01295	SN74LS86N
U53	1820-1997	7		IC FF TTL LS D-TYPE POS-EDGE-TRIG PRL-IN	01295	SN74LS374PC
U54	1820-2641	6	2	IC FF TTL LS D-TYPE POS-EDGE-TRIG PRL-IN	01295	SN74LS374N
U55	1820-2075	4	2	IC MISC TTL LS	01295	SN74LS245N
U56	1820-0629	0	2	IC FF TTL S J-K NEG-EDGE-TRIG	01295	SN74S112N
U57	1820-2102	8		IC LCH TTL LS D-TYPE OCTL	01295	SN74LS373N
U58	1820-2102	8		IC LCH TTL LS D-TYPE OCTL	01295	SN74LS373N
U61	1820-0535	7		IC DRVR TTL AND DUAL 2-INP	01295	SN75451BP
U62	1820-1211	8		IC GATE TTL LS EXCL-OR QUAD 2-INP	01295	SN74LS86N
U63	1820-1470	1		IC MUXR/DATA-SEL TTL LS 2-TO-1-LINE QUAD	01295	SN74LS157N
U64	1820-2641	6		IC FF TTL LS D-TYPE POS-EDGE-TRIG PRL-IN	01295	SN74LS374N
U65	1820-2075	4		IC MISC TTL LS	01295	SN74LS245N
U66	1820-1322	2	2	IC GATE TTL S NOR QUAD 2-INP	01295	SN74S02N
U67	1AF5-6202	3	1	I/O PROCESSOR CHIP	28480	1AF5-6202

Table 6-3. Replaceable Parts

Reference Designation	HP Part Number	C D	Qty	Description	Mfr Code	Mfr Part Number
U71	1820-0535	7	3	IC DRVR TTL AND DUAL 2-INP	01295	SN75451BP
U72	1820-1211	8		IC GATE TTL LS EXCL-OR QUAD 2-INP	01295	SN74LS86N
U73	1820-1470	1		IC MUXR/DATA-SEL TTL LS 2-TO-1-LINE QUAD	01295	SN74LS157N
U74	1820-1112	8		IC FF TTL LS D-TYPE POS-EDGE-TRIG	01295	SN74LS74N
U75	1820-1416	5		IC SCHMITT-TRIP TTL LS INV HEX 1-INP	01295	SN74LS14N
U76	1820-0681	4	2	IC GATE TTL 3 NAND QUAD 2-INP	01295	SN74S00N
U81	1820-0535	7		IC DRVR TTL AND DUAL 2-INP	01295	SN75451BP
U82	1820-1211	8		IC GATE TTL LS EXCL-OR QUAD 2-INP	01295	SN74LS86N
U83	1820-1997	7		IC FF TTL LS D-TYPE POS-EDGE-TRIG PRL-IN	01295	SN74LS374PC
U84	1820-1730	6		IC FF TTL LS D-TYPE POS-EDGE-TRIG COM	01295	SN74LS273N
U85	1820-1112	8		IC FF TTL LS D-TYPE POS-EDGE-TRIG	01295	SN74LS74N
U86	1820-0629	0		IC FF TTL S J-K NEG-EDGE-TRIG	01295	SN74S112N
U91	1820-0535	7		IC DRVR TTL AND DUAL 2-INP	01295	SN75451BP
U92	1820-1211	8		IC GATE TTL LS EXCL-OR QUAD 2-INP	01295	SN74LS86N
U93	1820-1730	6		IC FF TTL LS D-TYPE POS-EDGE-TRIG COM	01295	SN74LS273N
U94	1820-1197	9	2	IC GATE TTL LS NAND QUAD 2-INP	01295	SN74LS00N
U95	1820-1197	9		IC GATE TTL LS NAND QUAD 2-INP	01295	SN74LS00N
U96	1820-1451	8		IC GATE TTL S NAND QUAD 2-INP	01295	SN74S38N
U100	1820-0535	7		IC DRVR TTL AND DUAL 2-INP	01295	SN75451BP
U101	1820-0535	7		IC DRVR TTL AND DUAL 2-INP	01295	SN75451BP
U102	1820-1211	8		IC GATE TTL LS EXCL-OR QUAD 2-INP	01295	SN74LS86N
U103	1820-1201	6		IC GATE TTL LS AND QUAD 2-INP	01295	SN74LS08N
U104	1820-1211	8		IC GATE TTL LS EXCL-OR QUAD 2-INP	01295	SN74LS86N
U105	1820-1112	8		IC FF TTL LS D-TYPE POS-EDGE-TRIG	01295	SN74LS74N
U106	1820-0681	4		IC GATE TTL 3 NAND QUAD 2-INP	01295	SN74S00N
U107	1820-1449	4	1	IC GATE TTL S OR QUAD 2-INP	01295	SN74S32N
U108	1820-1633	8		IC BFR TTL S INV OCTL 1-INP	01295	SN74S240N
U116	1820-1633	8		IC BFR TTL S INV OCTL 1-INP	01295	SN74S240N
U117	1820-1322	2		IC GATE TTL S NOR QUAD 2-INP	01295	SN74S02N
U118	1820-1451	8		IC GATE TTL S NAND QUAD 2-INP	01295	SN74S38N
	0403-0289	3	2	EXTR-PC BD MED POLYC .063-RD-THKNS	28480	0403-0289
	1200-0639	8	3	SOCKET-IC 20-CONT DIP-SLDR	28480	1200-0639
	1200-0981	3	1	SOCKET-64-PIN	28480	1200-0981
	1480-0116	8	2	PIN-GRV .062-IN-DIA .25-IN-LG STL	28480	1480-0116

Table 6-4. Code List of Manufacturers

Mfr Code	Manufacturer Name	Address		Zip Code
01121	ALLEN-BRADLEY CO	MILWAUKEE	WI	53204
01295	TEXAS INSTR INC SEMICONDUCTOR DIV	DALLAS	TX	75222
24546	CORNING GLASS WORKS (BRADFORD)	BRADFORD	PA	16701
28480	HEWLETT-PACKARD CO CORPORATE HQ	PALO ALTO	CA	94304
73138	BECKMAN INSTRUMENTS INC. HELIPOT DIV	FULLERTON	CA	92634

SERVICING DIAGRAMS

SECTION

VII

7-1. INTRODUCTION

This section contains servicing diagrams for the HP 12006A Parallel Interface.

The content of this section is as follows:

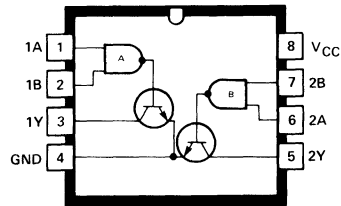
Figure 7-1. Integrated Circuit Base Diagrams

Figure 7-2. Parallel Interface Detailed Functional Block Diagram

Figure 7-3. Parallel Interface Parts Location Diagram

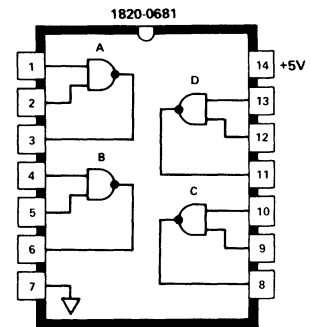
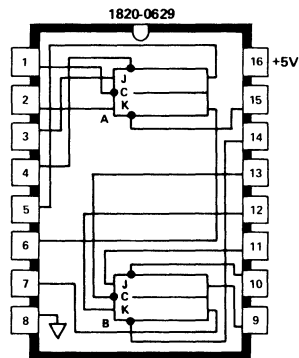
Figure 7-4. Parallel Interface Schematic Logic Diagram

1820-0535



INPUTS		OUTPUT
A	B	Y
H	H	H
L	H	L
L	L	L
H	L	L

INPUTS					OUTPUTS	
PRESET	CLEAR	CLOCK	J	K	Q	$\bar{Q}$
L	H	X	X	X	H	L
H	L	X	X	X	L	H
L	L	X	X	X	H*	H*
H	H	↓	L	L	Q ₀	$\bar{Q}_0$
H	H	↓	H	L	H	L
H	H	↓	L	H	L	H
H	H	↓	H	H	TOGGLE	
H	H	H	X	X	Q ₀	$\bar{Q}_0$



INPUTS					OUTPUTS	
PRESET	CLEAR	CLOCK	D		Q	$\bar{Q}$
L	H	X	X		H	L
H	L	X	X		L	H
L	L	X	X		H*	H*
H	H	↓	H		H	L
H	H	↓	L		L	H
H	H	L	X		Q ₀	$\bar{Q}_0$

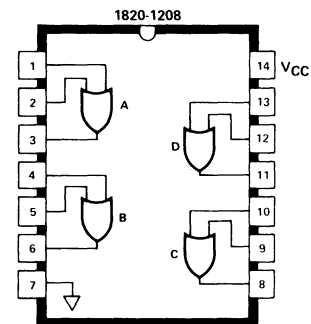
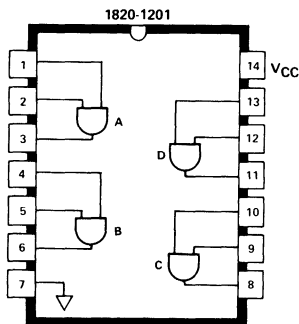
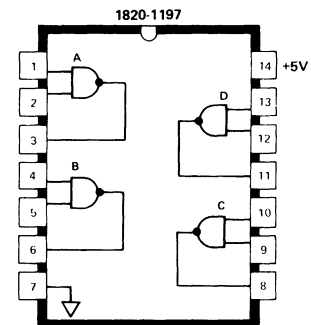
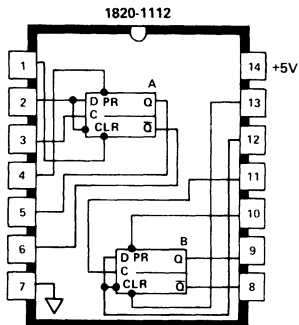
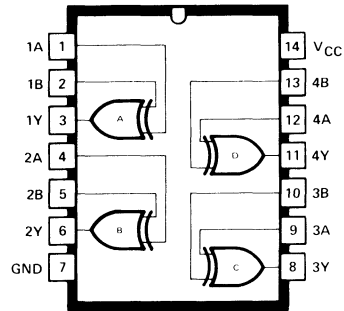


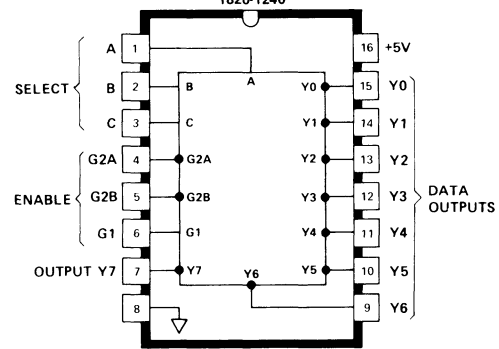
Figure 7-1. Integrated Circuit Base Diagrams (Sheet 1 of 5)

1820-1211

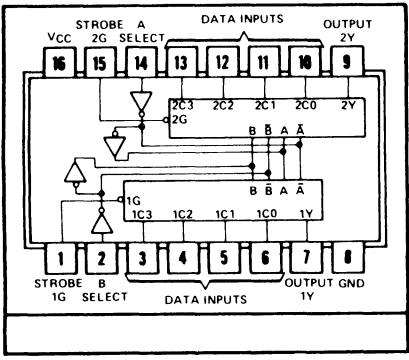
INPUTS		OUTPUT
A	B	Y
L	L	L
L	H	H
H	L	H
H	H	L



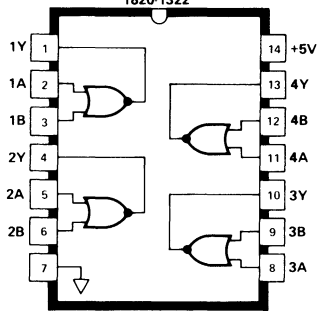
1820-1240



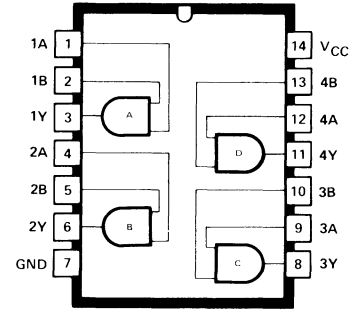
1820-1244



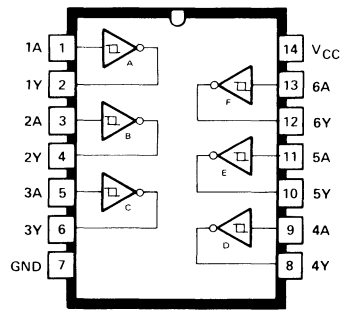
1820-1322



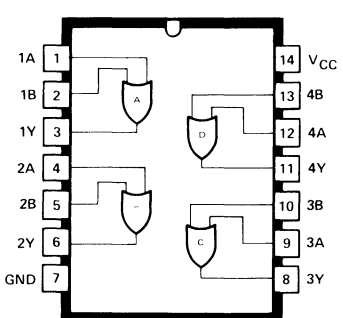
1820-1367



1820-1416



1820-1449



1820-1451

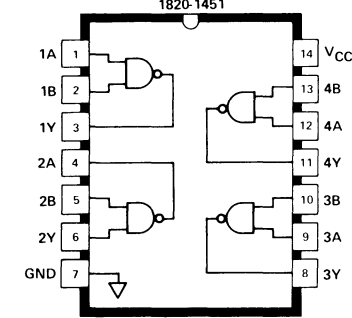


Figure 7-1. Integrated Circuit Base Diagrams (Sheet 2 of 5)

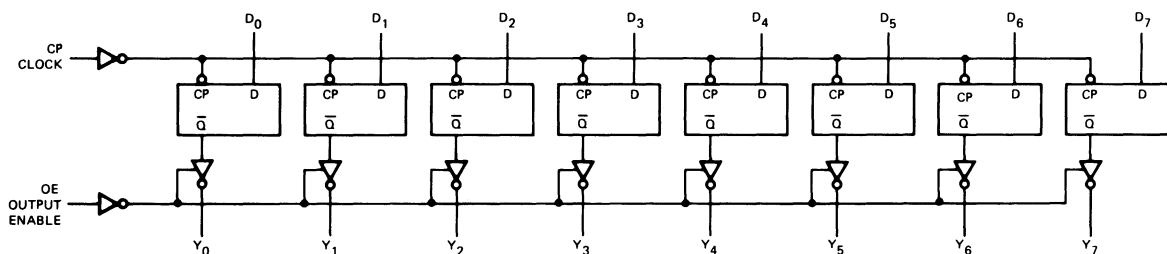
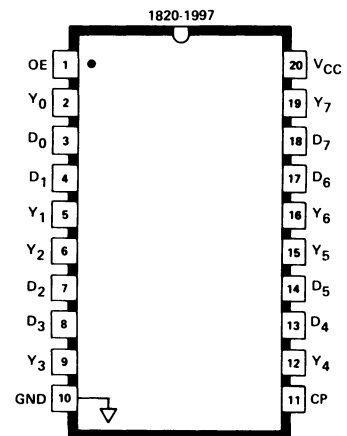
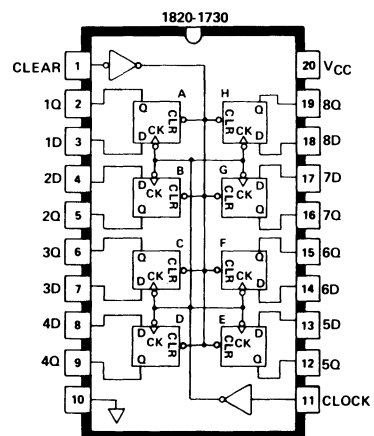
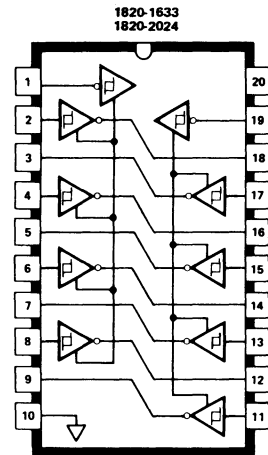
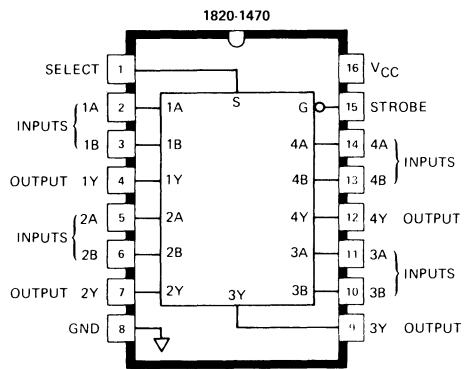


Figure 7-1. Integrated Circuit Base Diagrams (Sheet 3 of 5)

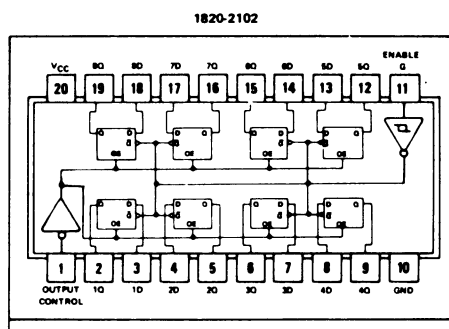
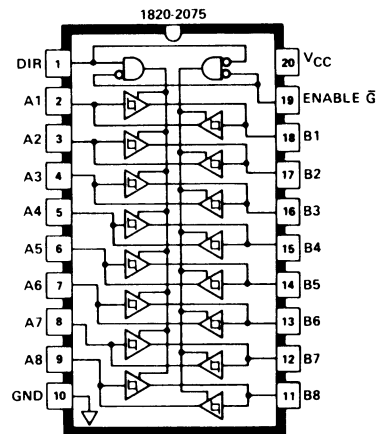
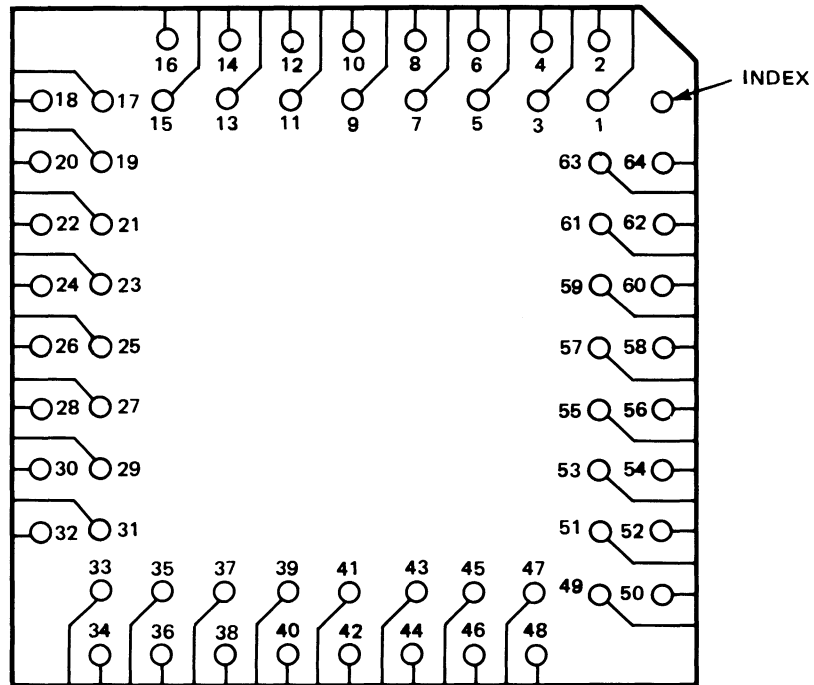


Figure 7-1. Integrated Circuit Base Diagrams (Sheet 4 of 5)

1AF5-6202

U67



1AF5-6202 I/O CHIP OUTLINE (COMPONENT SIDE)

PIN DEFINITIONS							
PIN	SIGNAL	PIN	SIGNAL	PIN	SIGNAL	PIN	SIGNAL
1	DMACYC-	17	GND	33	BRNI+	49	VCC
2	LDMAR+	18	VDD	34	CRS -	50	GND
3	SCEN-	19	CW1	35	IEN	51	VDD
4	REMOTE-	20	BCW2 +	36	DIAG	52	CB7 +
5	INTCYC +	21	BCW1 +	37	DVCMD	53	CB8 +
6	DMAEN	22	BCW0 +	38	PLSLV+	54	CB9 +
7	LOBYT	23	BVALID+	39	PON +	55	CB10 +
8	SACK	24	BIOGO+	40	SLACK +	56	CB11 +
9	NC	25	ICHID-	41	SLRQ+	57	CB12 +
10	SCLK +	26	BIAK+	42	CB0 +	58	CB13 +
11	LSBYT	27	CFF-	43	CB1 +	59	CB14 +
12	BPE+	28	PULIOR-	44	CB2 +	60	CB15 +
13	BMP-	29	IOEN	45	CB3 +	61	MEMGO+
14	CHSRQ-	30	IOCLK +	46	CB4 +	62	MRQ +
15	IRQ	31	PRDIS	47	CB5 +	63	NC
16	VCC	32	GND	48	CB6 +	64	GND

Figure 7-1. Integrated Circuit Base Diagrams (Sheet 5 of 5)

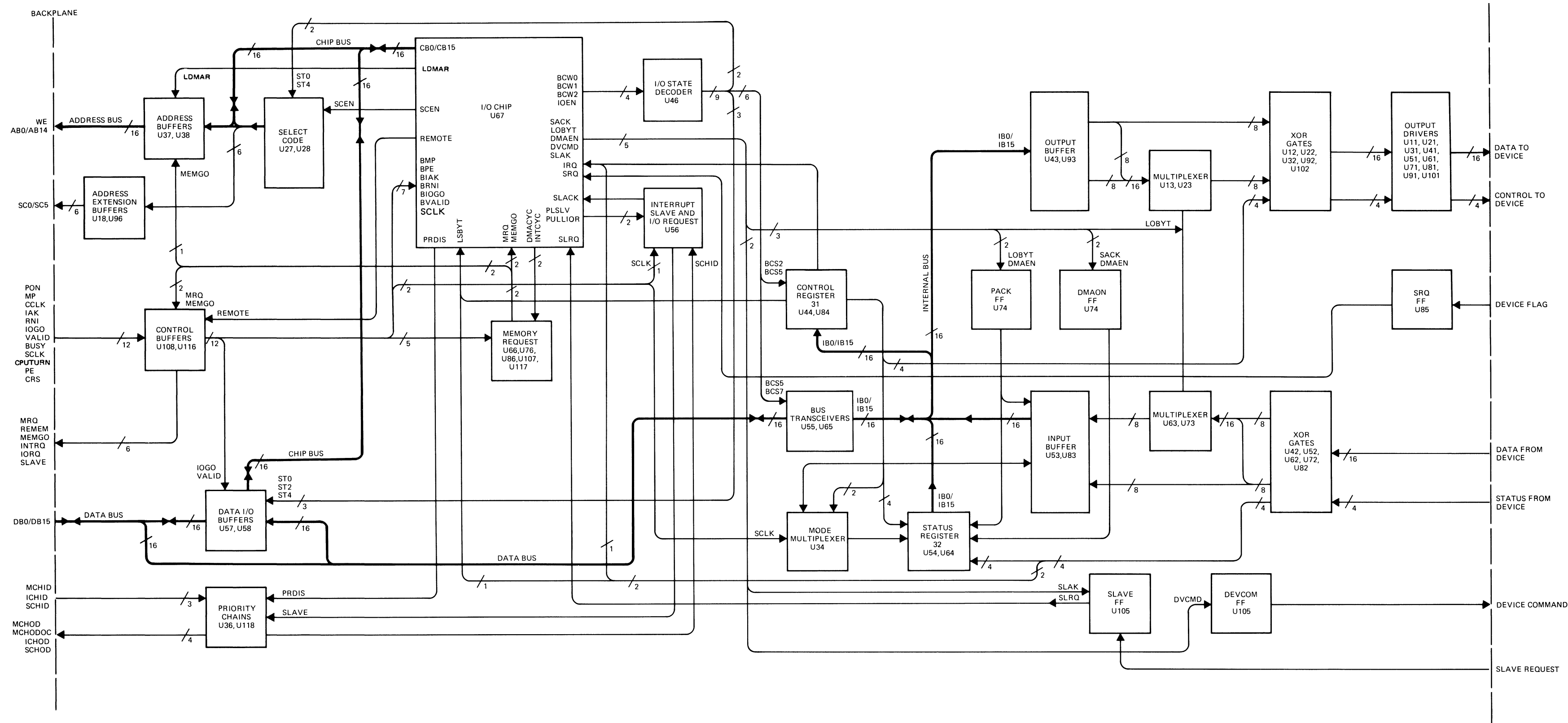


Figure 7-2. Parallel Interface Detailed Functional Block Diagram

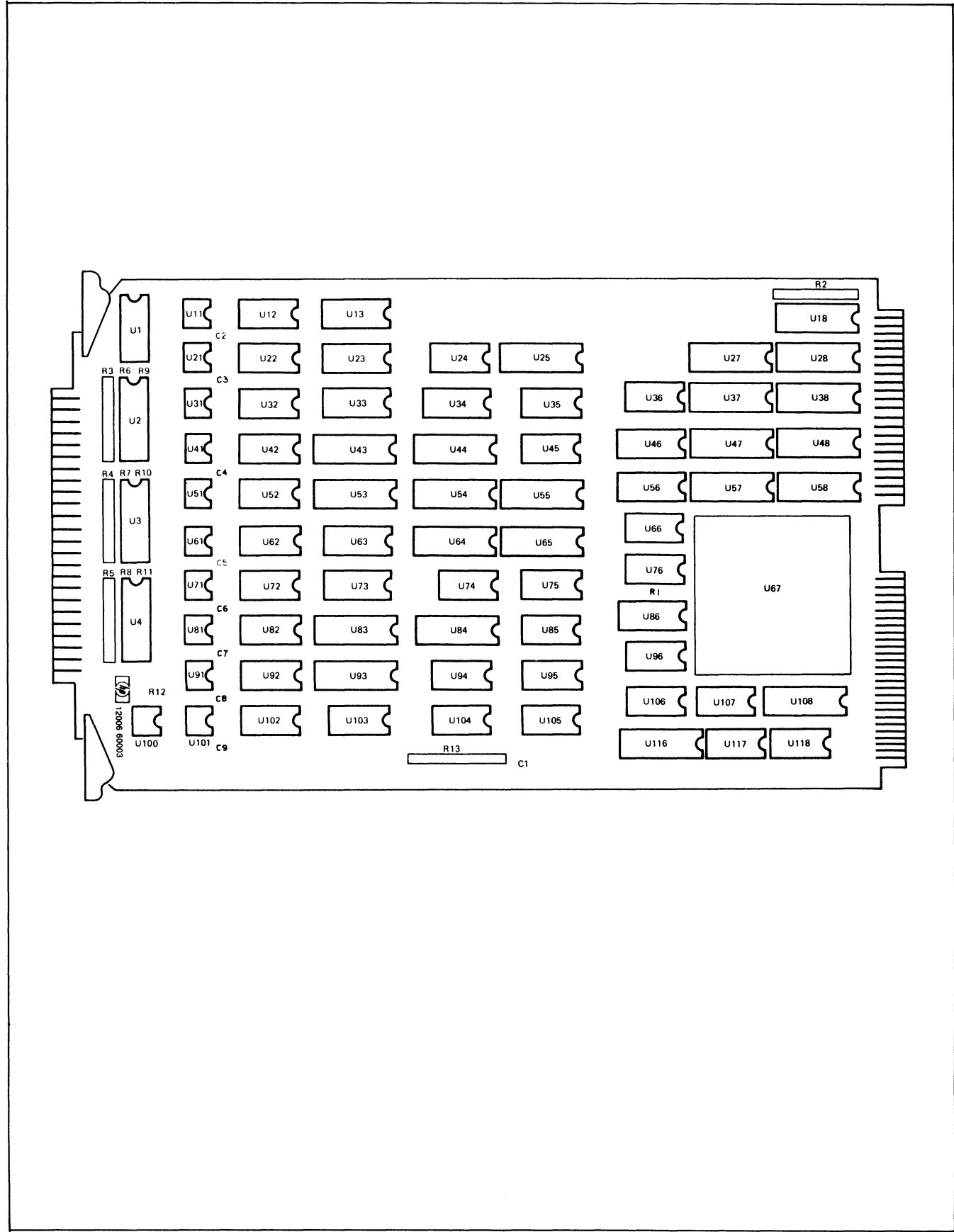


Figure 7-3. Parallel Interface Parts Location Diagram

Figure 7-4. Parallel Interface Schematic Logic Diagram (Sheet 2 of 2)

BACKDATING INFORMATION

SECTION

8

INTRODUCTION

This chapter provides a brief description of differences between Parallel Interface cards with different card assembly numbers and date codes.

Card Assembly 12006-60001

DATE CODE: B-2001

This version of the 12006A Parallel Interface card (PIC) had a large white Silicon-on-Sapphire (SOS) Input/Output Processor (IOP) at position U67. This IC (part number 1AC5-6001) was held in its socket by two spring clips.

WARNING

OBSERVE THE EYE-HAZARD SAFETY PRECAUTION if you work on this card's IOP. See the heading "Maintenance Differences" in this section for more information on servicing this card.

A description of the differences in the circuit for 12006-60001 follows. A copy of the 12006-60001 schematic is at the end of this section. The connections to a particular pin listed below replace the connections for that pin on the 12006-60003 schematic in section 7.

Sheet one of the schematic describes a functional block on the PIC called the IO Master. The IO Master section is common to all interface cards for A/L series computers. On sheet one of the schematic for B-2001, pins 4, 5, and 6 of U117 did not appear. The gate those pins are attached to was not used in that version of the PIC. There are other differences.

Many of the differences center around U86, which contains the MRQ and MEMGO flip-flops. On cards that have the date code B-2001, pins 14 and 15 of U86 were tied together and wired to pin 39 of U67, pin 3 of U116, pin 15 of U56 and becomes PDN+ (which is not connected). Pin 14 of U86 WAS NOT wired to pin 1 of U106. Pin 6 of U86 was tied to only pin 1 of U36. Finally, pins 9 and 12 of U86 were tied together and to pin 1 of U96, pin 61 of U67, and pins 2, 12, and 13 of U118.

On sheet two of the schematic, PICs with date code B-2001 differ from 12006-60003 because pins 3 and 4 of U34 WERE NOT wired to pin 11 of U104. Instead, pins 3, 4, 11, and 13 of U34 were only connected to pin 5 of U85.

Card Assembly 12006-60002

Parallel Interface cards made early in the production of the 12006-60002 were called HP 12006Bs. Some of the manuals also identified the product as a "B". The designation was later changed back to HP 12006A.

Card assembly 12006-60002 differs only slightly in physical layout from 12006-60003. Schematically they are the same except for some minor differences in the electrical values of components. The component differences are under the heading "Card Assembly 12006-60003". Component differences between card assembly 12006-60001 and -60002 are listed below.

Unless otherwise noted, the 12006-60002 and later versions of the PIC are more tolerant of asynchronous interrupts that might occur while a DMA (Direct Memory Access) is in progress.

DATE CODE: B-2042

The part numbers but not the electrical values of a few components changed with this date code. C1 changed to part number 0160-4825, C2 through C9 changed to part number 0160-4842, R1 changed to 0757-0280, and R12 changed to 0698-0082.

DATE CODE: A-2042

A-2042 came out after B-2042. PICs with the date code A-2042 had a different IOP at position U67. This new IOP had part number 1AF5-6001. The IOP socket did not change. The old IOP was part number 1AC5-6001.

WARNING

OBSERVE THE EYE-HAZARD SAFETY PRECAUTION if you work on this card's IOP. See the heading "Maintenance Differences" in this chapter for more information on servicing this card.

DATE CODE: A-2042a

The electrical values of two parts were changed. C1, which was a 560pf capacitor, was changed to a 470pf capacitor whose part number is 0160-4808. R12 was changed to a 464 ohm resistor which has part number 0757-0417. The old value was 562 ohms.

WARNING

OBSERVE THE EYE-HAZARD SAFETY PRECAUTION if you work on this card's IOP. See the heading "Maintenance Differences" in this chapter for more information on servicing this card.

Card Assembly 12006-60003

DATE CODE: A-2350

This is the current version of the Parallel Interface Card (PIC). The changes to the card from the previous assembly are a new I/O chip and socket at U67. The card was slightly modified to accept the new socket. Also, a required supplier for U54 and U64 was specified with special part numbers assigned to the parts.

The new I/O chip, part number 1AF5-6202, is an integrated circuit in a gray parallel in-line package (PIP). The special socket and adapter for the I/O chip is part number 1200-0981.

The part number for U54 and U64 is 1820-2641. Part number 1820-1997-T may also be used but 1820-1997 is not an acceptable replacement.

MAINTENANCE DIFFERENCES

All HP 12006As with the card assembly numbers of 12006-60001 and -60002 included a white SOS IOP as U67. The IOP was retained in a special socket by two spring-steel clips. In these versions of the card if the IO Processor passed testing but the card failed, only the card was returned for service. If only the IOP failed, only it was replaced.

The information on removing or installing the IOP is provided below if you need it. If you have a failure in a PIC or any other service problem, contact your nearest Hewlett-Packard Sales and Service Office for assistance. The Sales and Service Offices are listed in the back of this manual.

Removal and Installation of a white SOS IOP

Please read and understand all of the instructions for the procedure you are attempting before you start.

WARNING

Do not attempt to service the PIC while it is installed in the computer as you may receive a shock and/or damage the PIC and the computer.

Turn off the power to the computer and any peripheral attached to the PIC. Then disconnect any cable attached to PIC and remove the PIC from the card cage.

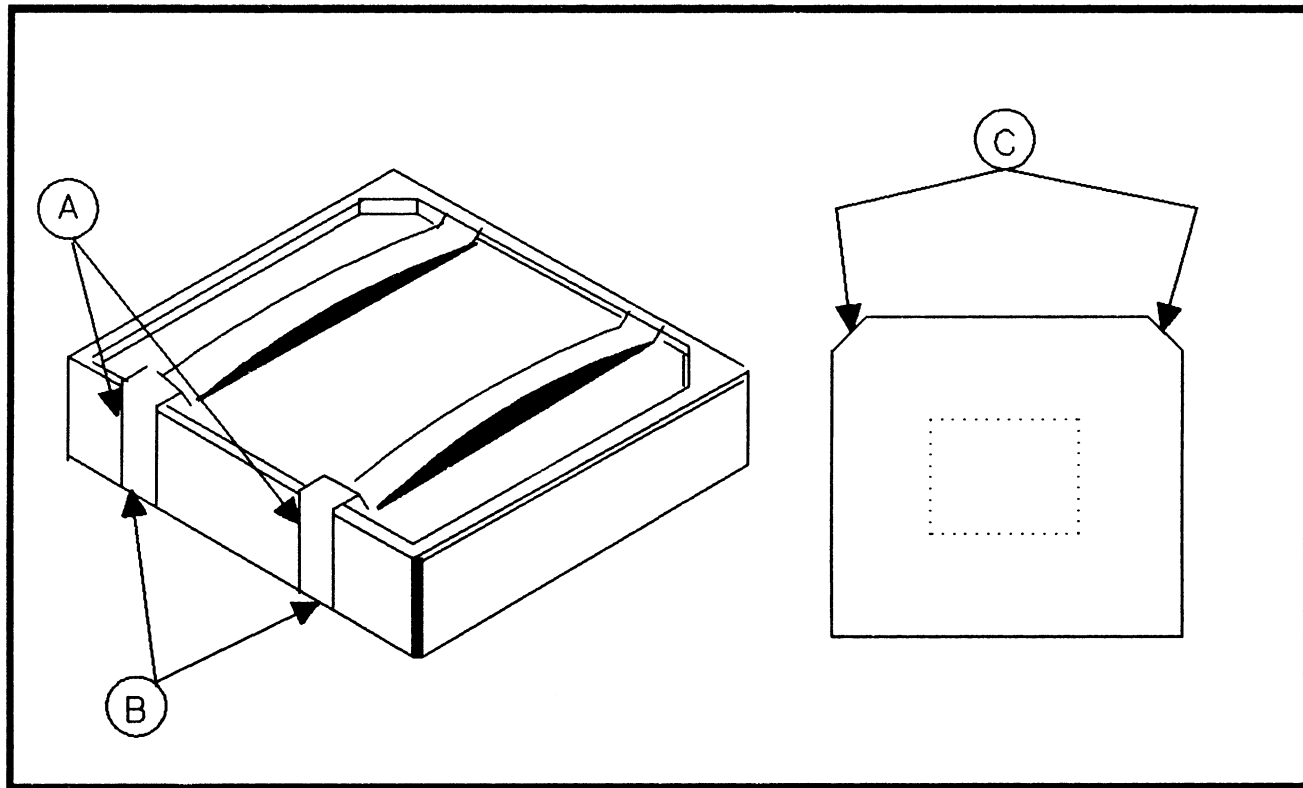


Figure 8-1. SOS Socket with chip and retaining clips.

WARNING

EYE-HAZARD SAFETY PRECAUTION - Wear safety glasses when removing or installing the retaining clips on the IOP. These clips are under tension and have sharp corners.

CAUTION

The IOP is sensitive to static-electric discharge. Follow the anti-static handling procedures in the front of this manual when removing or installing the IOP.

REMOVAL

- a. Remove the card from the computer and place it on a flat surface.
- b. While pressing down on one of the retaining clips with a thumb, insert the tip of a straight-blade screwdriver or similar tool between the retaining clip and the side of the socket at location A (see figure 8-1).
- c. Twist the screwdriver so the blade forces the clip free of the lip (B) on the side of the socket.
- d. When the retaining clip is free, lift it up and over the chip to free the clip from the slot in the socket.
- e. Remove the second clip by following steps b through d.
- f. Tip the card on edge and remove the chip. Carefully observe anti-static handling procedures when handling an IOP that has been removed from a card.

CAUTION

The spring clips exert enough force on the IOP socket to deform or damage it if no chip is installed. **DO NOT INSTALL THE SPRING CLIPS ON AN EMPTY SOCKET.**

INSTALLATION

- a. Place the card on a flat surface with the component side up.
- b. Locate both retaining clips.
- c. Place the chip in the socket, locating the two cut-off corners (C in figure 8-1) against the blocked-off corners of the socket. The trace side of the IOP must face down, toward the component side of the card, when the chip is placed in the socket.
- d. Place a retaining clip in one of the two slots provided for them in the side of the socket.
- e. Use a thumb to press down on the retaining clip while guiding it over the edge of the socket. Continue pressing down on the clip until it snaps over the lip (B in figure 8-1) on the side of the socket.
- f. Install the second clip in the same way you installed the first.

WARNING

To re-install the Parallel Interface Card (PIC) follow the installation instructions in section 2. Failure to install the PIC correctly may damage the card, the computer and/or injure you.

SUMMARY OF UPDATE

Section 1

The new Data Transfer Capabilities listed in the specifications are the results of tests of the PIC. The conditions of the test have also been stated.

Section 2

Revised wiring lists for cable construction replaced tables 2-3 and 2-4.

Section 3

A reference to the I/O Interfacing Guide was added in the Summary of I/O Instruction Usage paragraph. This manual provides a more detailed description of I/O instructions.

Section 4

No changes.

Section 5

The references to other manuals that cover diagnostics were brought up to date.

Section 6

The replaceable parts list was brought up to date.

Section 7

No changes.

Section 8

This new section contains backdating information for earlier versions of the card.

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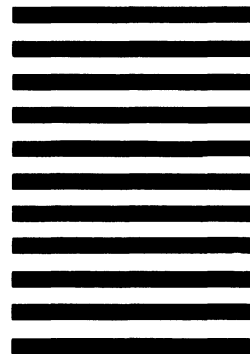
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Telex: 085/86 533 hpdd d

A,CH,CS,E,M,P

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Geschäftsstelle

Schleefstr. 28a

D-4600 DORTMUND-Aplerbeck

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A,CH,CM,CS,E,M,P

Hewlett-Packard GmbH

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D-6380 BAD HOMBURG

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D-2000 HAMBURG 60

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Telex: 0712816 HP ULM-D

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Arranged alphabetically by country

GREECE

Blue Star Ltd.

Blue Star Ltd.

Computation and Measurement

178, Kifissias Avenue
6th Floor
Halandri-ATHENS
Greece
Tel: 647 1673, 647 1543, 647 2971
A,CH,CM**,CS**,E,M,P
Kostas Karaynnis S.A.
8 Omirou Street
ATHENS 133
Tel: 32 30 303, 32 37 371
Telex: 215962 RKAR GR
A,CH,CM,CS,E,M,P
PLAISIO S.A.
Eliopoulos Brohers Ltd.
11854
ATHENS
Tel: 34-51-911
Telex: 216286
P

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IPESA
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GUATEMALA CITY
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Telex: 66678 HEWPA HX
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Telex: 85148 CET HX
CM
Schmidt & Co. (Hong Kong) Ltd.

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BANGALORE 560 025
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Telex: 0845-430
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Blue Star Ltd.
Band Box House
Prabhadevi
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Telex: 011-3751
Cable: BLUESTAR
A,M
Blue Star Ltd.
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414/2 Vir Savarkar Marg
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Cable: FROSTBLUE
A,CH*,CM,CS*,E,M
Blue Star Ltd.
Kalyan, 19 Vishwas Colony
Alkapuri, BORODA, 390 005
Tel: 65235
Cable: BLUE STAR
A
Blue Star Ltd.
7 Hare Street
CALCUTTA 700 001
Tel: 12-01-31
Telex: 021-7655
Cable: BLUESTAR
A,M
Blue Star Ltd.
133 Kodambakkam High Road
MADRAS 600 034
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Cable: BLUESTAR
A,M
Blue Star Ltd.
Bhandari House, 7th/8th Floors

Maruthankuzhi
TRIVANDRUM 695 013
Tel: 65799
Telex: 0884-259
Cable: BLUESTAR
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Computer Maintenance Corporation Ltd.
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CH**

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BERCA Indonesia P.T.
P.O.Box 496/Jkt.
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Telex: 46748 BERSAL IA
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P
BERCA Indonesia P.T.
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67060
TEL-AVIV
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Telex: 33569 Motil IL
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5



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Yokogawa-Hewlett-Packard Ltd.
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Photo & Cine Equipment
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Telex: 22247 MATIN KT
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P

W.J. Towell Computer Services
P.O. Box 75

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Telex: 30336 TOWELL KT
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Telex: 038 410
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A

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E

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P

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CASABLANCA
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AUCKLAND

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A,M

Northrop Instruments & Systems Ltd.

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NORTHERN IRELAND

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Telex: 3289 BROKER MB MUSCAT

P

Suhail & Saud Bahwan

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MUSCAT

Tel: 734 201-3

Telex: 3274 BAHWAN MB

E

Imtac LLC

P.O. Box 8676

MUTRAH

Tel: 601695

Telex: 5741 Tawoos On

A,C,M

PAKISTAN

Mushko & Company Ltd.

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Sector F-6/3

ISLAMABAD

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Cable: FEMUS Islamabad

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Mushko & Company Ltd.

Oosman Chambers

Abdullah Haroon Road

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Telex: 2894 MUSKO PK

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PANAMA

ElectroNico Balboa, S.A.

Calle Samuel Lewis, Ed. Alfa

Apartado 4929

PANAMA 5

Tel: 63-6613, 63-6748

Telex: 3483 ELECTRON PG

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PERU

Cía Electro Médica S.A.

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Casilla 1030

LIMA 1

Tel: 41-4325, 41-3703

Telex: Pub. Booth 25306

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SAMS

Rio De La Plata 305

SAN ISIDRO

Tel: 419928

Telex: 394 20450 PELIBERTAD

P

PHILIPPINES

The Online Advanced Systems

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Metro **MANILA**

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Telex: 63274 Online PN

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690-B Epifanio de los Santos

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Telex: 40018, 42000 ITT GLOBE MAC-

KAY BOOTH

P

PORTUGAL

Mundinter

Intercambio Mundial de ComAercio

S.A.R.L.

P.O. Box 2761

Av. Antonio Augusto de Aguiar 138

P-LISBON

Tel: (19) 53-21-31, 53-21-37

Telex: 16691 munter p

M

Soquimica

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1298 **LISBOA** Codex

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Telex: 13316 SABASA

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Telectra-Empresa Técnica de

Equipmentos Eléctricos S.A.R.L.

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P-LISBON 1

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Telex: 12598

CM,E

Rarcentro Ltda

R. Costa Cabral 575

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CH,CS

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QATAR

Computer Arabia

P.O. Box 2750

DOHA

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Telex: 4806 CHPARB

P

Nasser Trading & Contracting

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DOHA

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M

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Thuobah

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